may be involved in making modifications to applications Technical managers responsible for equipment purchase decisions Managers responsible for project planning Researchers involved in numerical algorithm development End users with an interest in understanding the performance of their applications While this publication is decidedly technical in nature, the fundamental concepts are presented from a user point of view and numerous examples are provided to reinforce these concepts. Furthermore, this publication is organized such that the information becomes more detailed as one progresses through the chapters. This organization will allow readers to stop, once they have achieved the level of understanding they desire, without having to search through the publication. To some extent, this book should be regarded as a series of subtopics that can be read alone

1 - 10 of **88** results* | **Next** ✦   **Publish date**

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S12	82	S S11 NOT 2003:2004
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S14	74	RD (unique items)
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S19	16	S S1 AND S3
S20	8	S S19 NOT PY=2003:2007
S21	3	RD (unique items)
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S23	1051	S (CACHE(1W)MISS??)(100N)(STATISTIC?? OR HEURISTIC? ? OR LOGARITHM?? OR WEIGHT??? OR MODEL??? OR MODEL??? OR METRICS OR FORMULA? ? OR SUM? ? OR EQUATION? ? OR QUANTITATIVE()ANALYSIS OR SAMPL??? OR ANALYTICAL)
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S25	25	S S1 AND S23
S26	3	S S24 NOT PY=2003:2007
S27	2	RD (unique items)
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[File 95] **TEME-Technology & Management** 1989-2007/Mar W2
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[File 420] **UnCover** 1988-2001/May 31
[File 434] **SciSearch(R) Cited Ref Sci** 1974-1989/Dec
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Subject summary

14/6/1 (Item 1 from file: 60) <u>Links</u>
0000282649   IP Accession No: 93686
Memory master-class
Publication Date: 1999

14/6/2 (Item 1 from file: 56) <u>Links</u>
0000589443   IP Accession No: 200701-90-001189
Intel looks to nanotechnology
Publication Date: 2005

14/6/3 (Item 2 from file: 56) <u>Links</u>
0000194451   IP Accession No: 0004362
Built-in-self-test considerations in a high-performance, general-purpose processor.
Publication Date: 1992

14/6/4 (Item 3 from file: 56) <u>Links</u>
0000149283   IP Accession No: 1927611
Programming style on the IBM 3090 Vector Facility considering both performance and flexibility.
Publication Date: 1988

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0000124435   IP Accession No: 1675876
Mainframe tuning in the high-MIPS era.
Publication Date: 1987

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Tandy 600 and the Tandy 3000.
Publication Date: 1985

14/6/7 (Item 6 from file: 56) <u>Links</u>
0000084620   IP Accession No: 1248991
Computerised collation.
Publication Date: 1985

14/6/8 (Item 1 from file: 35) <u>Links</u>
01483763   ORDER NO: AADAA-I9615748
PROJECTIVE BLOCK LANCZOS ALGORITHM AND ITS PARALLELIZATION ON DISTRIBUTED-MEMORY
PARALLEL PROCESSORS
Year: 1995

14/6/9 (Item 2 from file: 35) <u>Links</u>
01228245   ORDER NO: AADMM-61804
A COMPUTERIZED DATA ACQUISITION AND CONTROL SYSTEM FOR FABRY-PEROT INTERFEROMETRY
Year: 1990

14/6/10 (Item 3 from file: 35) <u>Links</u>
01167313   ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
BEPLASY: PC-BASED PLANNING MODEL FOR FARMS
Original Title: BEPLASY: EIN BETRIEBSPLANUNGSSYSTEM FUR LANDWIRTSCHAFTSBETRIEBE AUF DEM PC
Year: 1991

14/6/11 (Item 1 from file: 8) <u>Links</u>
10049771
Title: A framework for profiling multiprocessor memory performance
Conference Title: Proceedings - Tenth International Conference on Parallel and Distributed Systems (ICPADS 2004)
Publication Year: 2004

14/6/12 (Item 2 from file: 8) <u>Links</u>
09822688
Title: Multi-mode SAR data processor for satellite and airborne systems
Conference Title: SAR Image Analysis, Modeling, and Techniques VI
Publication Year: 2004

14/6/13 (Item 3 from file: 8) <u>Links</u>
05937013
Title: Query optimization in a memory-resident domain relational calculus database system.
Publication Year: 1990

14/6/14 (Item 4 from file: 8) <u>Links</u>
05771478
Title: Modification of IBM-PC Data Acquisition and Control Adaptor for versatile data acquisition and control system.
Publication Year: 1989

14/6/15 (Item 5 from file: 8) <u>Links</u>
05684575
Title: ULTIMATE SPEED-UP: BEING A TREATISE ON THE SIEVE OF ERATOSTHENES.
Publication Year: 1988

14/6/16 (Item 6 from file: 8) <u>Links</u>
04889099
Title: APPLICABILITY OF GROUNDWATER MODELS TO MICROCOMPUTERS.
Conference Title: Hydraulics and Hydrology in the Small Computer Age, Proceedings of the Specialty Conference.
Publication Year: 1985

14/6/17 (Item 7 from file: 8) <u>Links</u>
04800879
Title: IBM SERIES/1 FIELD UPGRADE TO PROVIDE FASTER PROCESSING AND INCREASED MEMORY CAPACITY.
Publication Year: 1985

14/6/18 (Item 8 from file: 8) <u>Links</u>
03996768
Title: DEVELOPMENT OF DIPS MASS MEMORY SYSTEM.
Publication Year: 1980

14/6/19 (Item 1 from file: 583) <u>Links</u>
09381763
Ease-of-use from the NetVista desktop family
ASEAN: IBM UNVEILS NEW DESKTOP COMPUTERS
Sep 2000

14/6/20 (Item 2 from file: 583) <u>Links</u>
09310040
IBM unveils NetVista line of desktop PCs
SINGAPORE: IBM UNVEILS DESKTOP PCs
19 Jun 2000

14/6/21 (Item 3 from file: 583) <u>Links</u>
09054772
IBM's 1998 sales and purchases in Taiwan hitNT$100 billion
TAIWAN: IBM CONTINUES TO EXPAND IN TAIWAN
03 Feb 1999

14/6/22 (Item 4 from file: 583) <u>Links</u>
06372722
Notebook computing today and tomorrow
WORLD: NOTEBOOKS OF TOMORROW
02 Oct 1996

14/6/23 (Item 5 from file: 583) <u>Links</u>
05120785
Just wild about gatway cards
UK - DATAHOUSE LAUNCHES RANGE OF GATEWAY CARDS
0 May 1992

14/6/24 (Item 6 from file: 583) <u>Links</u>
04368591
HIGH END AS/400 FAR EXCEEDS EARLIER MODEL
US - HIGH END AS/400 FAR EXCEEDS EARLIER MODEL
0 June 1991

14/6/25 (Item 7 from file: 583) <u>Links</u>
04324052
CALCULUS HAS BOARD AND SOFTWARE FOR FAX CAPABILITY
US - CALCULUS HAS BOARD AND SOFTWARE FOR FAX CAPABILITY
11 June 1991

14/6/26 (Item 8 from file: 583) <u>Links</u>
04314408
DOLCH LAUNCHES 33MHz 486 PC
UK - DOLCH LAUNCHES 33MHz 486 PC
28 May 1991

14/6/27 (Item 9 from file: 583) <u>Links</u>
04226397
IBM EASES RS/6000 THREAT WITH AS/400 PRICE CUTS
UK - IBM EASES RS/6000 THREAT WITH AS/400 PRICE CUTS
23 April 1991

14/6/28 (Item 10 from file: 583) <u>Links</u>
03446632
DATA GENERAL INTRODUCES MINI TO RIVAL DEC AND IBM
US - DATA GENERAL INTRODUCES MINI TO RIVAL DEC AND IBM
26 April 1990

14/6/29 (Item 11 from file: 583) <u>Links</u>
03442516
AEG TO LAUNCH NEW PC RANGE
UK - AEG TO LAUNCH NEW PC RANGE
0 April 1990

14/6/30 (Item 12 from file: 583) <u>Links</u>
03400021
WEBER TO INVEST IN DATA PROCESSING
BRAZIL - WEBER TO INVEST IN DATA PROCESSING
19 February 1990

14/6/31 (Item 13 from file: 583) <u>Links</u>
03370090
ITALIAN FIRMS RETURN
S AFRICA - ITALIAN FIRMS RETURN
19 March 1990

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03106658
BANK AWARDS SOFTWARE CONTRACT
HUNGARY - BANK AWARDS SOFTWARE CONTRACT
21 December 1989

14/6/33 (Item 15 from file: 583) <u>Links</u>
03106446
CTL DEVELOPS COMPUTER WHICH UNDERSTANDS SPANISH
SPAIN - CTL DEVELOPS COMPUTER WHICH UNDERSTANDS SPANISH
6 December 1989

14/6/34 (Item 16 from file: 583) <u>Links</u>
02560301
AMDAHL LAUNCHES ENHANCED VERSION OF MAINFRAME UNIX
US - AMDAHL LAUNCHES ENHANCED VERSION OF MAINFRAME UNIX
20 February 1989

14/6/35 (Item 17 from file: 583) <u>Links</u>
00072314
IBM REORGANISES SYSTEM 36 RANGE
UK - IBM REORGANISES SYSTEM 36 RANGE
30 January 1986

14/6/36 (Item 1 from file: 2) <u>Links</u>
07549166   INSPEC Abstract Number: C2000-05-6150C-012
Title: An interleaving transformation for parallelizing reductions for distributed-memory parallel machines
Publication Date: March 2000
  Copyright 2000, IEE

14/6/37 (Item 2 from file: 2) <u>Links</u>
07349135
Title: The age of obsolescence [notebook computer upgrades]
Publication Date: 19 July 1999

14/6/38 (Item 3 from file: 2) <u>Links</u>
05720163   INSPEC Abstract Number: C9409-6150J-006
Title: Software development DOS 6.3
Publication Date: 1994

14/6/39 (Item 4 from file: 2) <u>Links</u>
05705868   INSPEC Abstract Number: C9408-6160D-019
Title: Locking and latching in a memory-resident database system
Publication Date: 1992

14/6/40 (Item 5 from file: 2) <u>Links</u>
05494089   INSPEC Abstract Number: B9311-1265D-017, C9311-5320G-013
Title: ECC design of a custom DRAM storage unit
Publication Date: 1993

14/6/41 (Item 6 from file: 2) <u>Links</u>
04661079   INSPEC Abstract Number: C90047391
Title: Query optimization in a memory-resident domain relational calculus database system
Publication Date: March 1990

14/6/42 (Item 7 from file: 2) <u>Links</u>
04525448   INSPEC Abstract Number: C90007094
Title: PowerFlex: a versatile, upgradable AT clone
Publication Date: Nov. 1989

14/6/43 (Item 8 from file: 2) <u>Links</u>
04423037   INSPEC Abstract Number: B89051887, C89050736
Title: A high-speed multichannel neural data acquisition system for IBM PC compatibles
Publication Date: Jan. 1989

14/6/44 (Item 9 from file: 2) <u>Links</u>
04231936   INSPEC Abstract Number: D88002768
Title: Electronic typewriters: what's new in 1988?
Publication Date: 28 July 1988

14/6/45 (Item 10 from file: 2) <u>Links</u>
04143465   INSPEC Abstract Number: C88034860
Title: Fixed disk accelerator: awesome I/O board lightning fast
Publication Date: March 1988

14/6/46 (Item 11 from file: 2) <u>Links</u>
04025995   INSPEC Abstract Number: C88004915
Title: Roots II (genealogy package)
Publication Date: Fall 1987

14/6/47 (Item 12 from file: 2) <u>Links</u>
03697949   INSPEC Abstract Number: D86001963
Title: Compaq's Portable II, Portable 286, and DeskPro 286 personal computers
Publication Date: March 1986

14/6/48 (Item 13 from file: 2) <u>Links</u>
03564317   INSPEC Abstract Number: C86003474
Title: Goupil G4
Publication Date: Sept. 1985

14/6/49 (Item 14 from file: 2) <u>Links</u>
03521824   INSPEC Abstract Number: C85045729
Title: New performance classes: Compaq Deskpro 286 (microcomputer)
Publication Date: July 1985

14/6/50 (Item 15 from file: 2) <u>Links</u>
03423213   INSPEC Abstract Number: C85019495
Title: Ericsson PC: IBM PC-compatible-but competitive?
Publication Date: Oct. 1984

14/6/51 (Item 16 from file: 2) <u>Links</u>
03371324   INSPEC Abstract Number: C85006323
Title: NEC APC III

Publication Date: Oct. 1984

14/6/52 (Item 17 from file: 2) Links
03354475 INSPEC Abstract Number: C85002129, D84003154
Title: The IBM PC AT
Publication Date: Oct. 1984

14/6/53 (Item 18 from file: 2) Links
03338059 INSPEC Abstract Number: C84050101, D84002938
Title: IBM's new personal computer
Publication Date: Sept. 1984

14/6/54 (Item 19 from file: 2) Links
03301781 INSPEC Abstract Number: C84039137
Title: The expanding realm of the IBM PC
Publication Date: Feb. 1984

14/6/55 (Item 20 from file: 2) Links
03270208 INSPEC Abstract Number: C84029968, D84001632
Title: IBM's new Sys/36
Publication Date: 15 May 1984

14/6/56 (Item 21 from file: 2) Links
03236966 INSPEC Abstract Number: C84021909
Title: Build this typewriter-to-computer interface. III
Publication Date: Feb. 1984

14/6/57 (Item 22 from file: 2) Links
03235815 INSPEC Abstract Number: C84019808, D84001096
Title: Portable-a mixed bag
Publication Date: April 1984

14/6/58 (Item 23 from file: 2) Links
02289566 INSPEC Abstract Number: B79004590, C79001670
Title: From nanosecond to picosecond (Josephson-junction memories)
Publication Date: 1978

14/6/59 (Item 1 from file: 6) Links
  Fulltext available through: Check for PDF Download Availability and Purchase
2011712   NTIS Accession Number: N19970010150
Aerodynamic Optimization of the High Speed Civil Transport
(Final Report)
Oct 96

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1952915   NTIS Accession Number: DE96004812
Real-time MPEG software decoder using a portable message-passing library
1995

14/6/61 (Item 1 from file: 256) Links
02760722   Document Type: Company
Division Name: IBM TJ Watson Research Center
IBM Corp (760722)
Revision Date: 00000000

14/6/62 (Item 2 from file: 256) Links
00155026   Document Type: Review
Product Names: Artificial Intelligence (830217)
Title: AI's Next Brain Wave Apr 25, 2005
Revision Date: 20070300

14/6/63 (Item 3 from file: 256) Links
00147072   Document Type: Review
Product Names: JBuilder 9 (651991)
Title: JBuilder's gains impressive Jun 2, 2003
Revision Date: 20030830

14/6/64 (Item 4 from file: 256) Links
00140432   Document Type: Review

Product Names: AIX 5L (695947); Solaris 9 (334707)
Title: IBM, Sun Update Unix Versions Jul 2002
Revision Date: 20021030

14/6/65 (Item 1 from file: 95) <u>Links</u>
01051863 E96111359310
Rewritable optical disk drive technology
(Wiederbeschreibbare optische Disk-Technik) , 1996

14/6/66 (Item 2 from file: 95) <u>Links</u>
00951592 E95120420310
Properties of delay-cost scheduling in time-sharing systems
(Eigenschaften des Verzoegerungs-Kosten-Ablaufs in Zeit-Teilungssystemen) , 1995

14/6/67 (Item 3 from file: 95) <u>Links</u>
00832926 E94111069310
Der 64-Mbit-DRAM - ein Speicherbaustein fuer das 21. Jahrhundert
, 1994

14/6/68 (Item 1 from file: 99) <u>Links</u>
2179000 H.W. Wilson Record Number: BAST95053970
Data-compression chips get application-specific
19950800

14/6/69 (Item 2 from file: 99) <u>Links</u>
1731816 H.W. Wilson Record Number: BAST93006685
The low-end workstation race
Augmented Title: buyer's guide
19930115

14/6/70 (Item 3 from file: 99) <u>Links</u>
1415252 H.W. Wilson Record Number: BAST93040757
HDS delivers improved drives
Augmented Title: Hitachi's 7600 disk storage subsystem
19930815

14/6/71 (Item 4 from file: 99) <u>Links</u>
0897575 H.W. Wilson Record Number: BAST90023860
IBM boosts memory and logic density
19900412

14/6/72 (Item 5 from file: 99) <u>Links</u>
0562358 H.W. Wilson Record Number: BAST84055308
Thomson enters DRAM business with boost from Oki and IBM
19841008

14/6/73 (Item 1 from file: 420) <u>Links</u>
13199603 UnCover No.: 251117113171
News.
August 1, 1999 ,

14/6/74 (Item 1 from file: 34) <u>Links</u>
08406074 Genuine Article#: 282AZ Number of References: 23
An interleaving transformation for parallelizing reductions for distributed-memory parallel machines
(ABSTRACT AVAILABLE)
Publication date: 20000200

21/3,K/1 (Item 1 from file: 56) <u>Links</u>
Computer and Information Systems Abstracts
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0000299743   IP Accession No: 0271975
Message proxies for efficient, protected communication on SMP clusters
Lim, Beng-Hong; Heidelberger, Philip; Pattnaik, Pratap; Snir, Marc IBM T.J. Watson Research Cent, Yorktown Heights, NY, USA
Pages: 116-127
Publication Date: 1997
Publisher: IEEE, LOS ALAMITOS, CA, (USA)
Conference:
The 1997 3rd International Symposium on High-Performance Computer Architecture, HPCA , San Antonio, TX , USA , 01-05 Feb. 1997
Document Type: Conference Paper
Record Type: Abstract
Language: English
File Segment: Computer & Information Systems Abstracts
...to run a message proxy, a communication process that provides protected access to the network. We implement message proxy based communication between a pair of **IBM** Model G30 SMPs and analyze the resulting overheads. We derive a performance model that shows that cache-miss latency within an SMP influences message proxy... ...custom hardware for three of the ten applications, and are between 10-30% slower for the other seven applications. A direct cache-update mechanism to **reduce cache misses** improves the performance of message proxies on communication-intensive programs by 7-25%. We conclude that message proxies provide a viable alternative to custom hardware...

21/3,K/2 (Item 1 from file: 8) <u>Links</u>
   Fulltext available through: <u>USPTO Full Text Retrieval Options</u>
Ei Compendex(R)
(c) 2007 Elsevier Eng. Info. Inc. All rights reserved.
06968263   **E.I. No:** EIP94111439301
Title: Improving performance of linear algebra algorithms for dense matrices, using algorithmic prefetch
Author: Agarwal, R.C.; Gustavson, F.G.; Zubair, M.
Source: IBM Journal of Research and Development v 38 n 3 May 1994. p 265-275
Publication Year: 1994
CODEN: IBMJAE **ISSN:** 0018-8646
Language: English
Abstract: In this paper, we introduce a concept called algorithmic prefetching, for exploiting some of the features of the **IBM** RISC System/6000 computer. Algorithmic prefetching denotes changing algorithm A to algorithm B, which contains additional steps to move data from slower levels of memory to faster levels, with the aim that algorithm B outperform algorithm A. The objective of algorithmic prefetching is to **minimize** any penalty due to **cache misses** in the innermost loop of an algorithm. This concept, along with ?cache blocking,' can be exploited to improve the performance of linear algebra algorithms for...
Identifiers: Algorithmic prefetch; **International Business Machines** RISC System/6000; Cache blocking

21/3,K/3 (Item 1 from file: 2) <u>Links</u>
INSPEC
(c) 2007 Institution of Electrical Engineers. All rights reserved.
06376112 **INSPEC Abstract Number:** C9610-5470-027
Title: A three-parameter fast Givens QR algorithm for superscalar processors
Author Carrig, J.J., Jr.; Meyer, G.G.L.
Author Affiliation: Dept. of Electr. & Comput. Eng., Johns Hopkins Univ., Baltimore, MD, USA
Conference Title: Proceedings of the 1996 International Conference on Parallel Processing. Vol.2 Algorithms and Applications Part vol.2   p. 11-18 vol.2
Editor(s): Bojanczyk, A.
Publisher: IEEE Comput. Soc. Press , Los Alamitos, CA, USA
Publication Date: 1996 **Country of Publication:** USA   3 vol. (xvi+278+xv+173+230) pp.
ISBN: 0 8186 7623 X   **Material Identity Number:** XX96-02685
 Conference Title: Proceedings of 25th International Conference on Parallel Processing
Conference Sponsor: Int. Assoc. Comput. & Commun.; Pennsylvania State Univ
Conference Date: 12-16 Aug. 1996   **Conference Location:** Ithaca, NY, USA
Language: English
 Subfile: C
Abstract: ...superscalar processors. We provide a selection of parameter values for which the new algorithm reduces to the standard algorithm, but show that non-standard values **minimize** the number of **cache misses**, memory references and pipeline stalls. Using a tractable model of a superscalar machine architecture, we derive rules for estimating the optimal combination of parameter values... ...a speedup over the standard algorithm of 2.4 on the Intel Pentium Pro system, 2.0 on a single thin POWER2 processor of the **IBM** SP2, 1.6 on a single wide POWER2 processor of the **IBM** SP2, and 4.2 on a single R8000 processor of the SGI POWER Challenge XL.
Identifiers: ...IBM SP2

27/3,K/1 (Item 1 from file: 56) <u>Links</u>
  Fulltext available through: <u>Institute of Electrical and Electronics Engineers</u>   <u>USPTO Full Text Retrieval Options</u>
Computer and Information Systems Abstracts
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0000338438   IP Accession No: 402971
System optimization for OLTP workloads
Kunkel, Steven; Armstrong, Bill; Vitale, Philip IBM, Rochester, MN, USA
IEEE Micro , v 19 , n 3 , p 56-64 , 1999
Publication Date: 1999
Publisher: IEEE, LOS ALAMITOS, CA, (USA)
Document Type: Journal Article
Record Type: Abstract
Language: English
ISSN: 0272-1732
File Segment: Computer & Information Systems Abstracts
Abstract:
In 1995, the **IBM** AS/400 changed the architecture of its microprocessors to a 64-bit PowerPC AS processor. This conversion from CISC to RISC precipitated a large software... ...entire OS/400 operating system. Many new tools and techniques were developed to optimize the interaction of hardware and software. By improving the compiler with **profiling** information, reducing pathlength through critical paths, reducing **cache misses** and snoop-hit-modified misses, and avoiding unnecessary task dispatches, system performance and scalability were significantly improved.

 27/3,K/2 (Item 1 from file: 35) <u>Links</u>
Dissertation Abs Online
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01379842   ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
PERFORMANCE IMPACT OF SHARED MEMORY LATENCY IN MULTIPROCESSORS: MODELS AND EXPERIMENTS
Author: BRORSSON, MATS
Degree: TEKN.DR
Year: 1994
Corporate Source/Institution: LUNDS UNIVERSITET (SWEDEN) (0899)
Source: Volume 5504C of Dissertations Abstracts International.
PAGE 1264 . 20 PAGES
Location of Reference Copy: DEPARTMENT OF COMPUTER ENGINEERING, LUND UNIVERSITY, P.O. BOX 118, S-221 00 LUND, SWEDEN
   ...techniques are presented. An analytic model of single-program-multiple-data program execution time has been used to explain the execution time measurements on the **IBM** RP3 experimental multiprocessor. The model is shown to be useful to predict execution times divided in serial section, parallel section and linear contention execution times... ...which was developed in order to carry out accurate measurements of the performance impact of various cache coherence policies. The program-driven simulation technique uses **interpretation** of instructions in simulated processors. This technique is shown to be effective in comparison to other state-of-the-art techniques, such as execution-driven...
...demonstrate that performance bottlenecks are easily spotted with the visual model.
   The visual model has been refined in order to quantitatively predict the number of **cache misses** for different access categories. Architectural simulations have been used to verify the accuracy of the quantitative model. The number of cold, coherence and directory replacement...

29/3,K/1 (Item 1 from file: 56) <u>Links</u>
Computer and Information Systems Abstracts
0000299743   IP Accession No: 0271975
Message proxies for efficient, protected communication on SMP clusters
Lim, Beng-Hong; Heidelberger, Philip; Pattnaik, Pratap; Snir, Marc IBM T.J. Watson Research Cent, Yorktown Heights,
NY, USA
Pages: 116-127
Publication Date: 1997
Publisher: IEEE, LOS ALAMITOS, CA, (USA)
Conference:
The 1997 3rd International Symposium on High-Performance Computer Architecture, HPCA , San Antonio, TX , USA , 01-
05 Feb. 1997
Document Type: Conference Paper
Record Type: Abstract
Language: English
File Segment: Computer & Information Systems Abstracts
Abstract:
...to run a message proxy, a communication process that provides protected access to the network. We implement
message proxy based communication between a pair of **IBM Model** G30 SMPs and analyze the resulting overheads. We
derive a performance **model** that shows that **cache-miss** latency within an SMP influences message proxy performance
significantly. Simulations of a suite of ten parallel applications demonstrate that message proxies match the performance
of... ...hardware for three of the ten applications, and are between 10-30% slower for the other seven applications. A direct
cache-update mechanism to reduce **cache misses** improves the performance of message proxies on communication-
intensive programs by 7-25%. We conclude that message proxies provide a viable alternative to custom hardware...

29/3,K/2 (Item 2 from file: 56) <u>Links</u>
   Fulltext available through: <u>USPTO Full Text Retrieval Options</u>
Computer and Information Systems Abstracts
0000293072   IP Accession No: 0279235
Accuracy and speed-up of parallel trace-driven architectural simulation
Nguyen, A-T; Bose, P; Ekanadham, K; Nanda, A; Michael, M IBM Thomas J. Watson Research Cent, Yorktown Heights,
NY, USA
PROC INT PARALL PROCESS SYMP IPPS , p 39-44 , 1997
Publication Date: 1997
Publisher: IEEE, LOS ALAMITOS, CA, (USA)
Conference:
The 1997 11th International Parallel Processing Symposium, IPPS 97 , Geneva , Switz , 01-05 Apr. 1997
Document Type: Conference Paper; Journal Article
Record Type: Abstract
Language: English
ISSN: 1063-7133
File Segment: Computer & Information Systems Abstracts
Abstract:
...performance processor-memory sub-systems. In this paper, we examine the varying speed-up opportunities available
by processing a given trace in parallel on an **IBM** SP-2 machine. We also develop a simple, yet effective method of
correcting for cold-start **cache miss** errors, by the use of overlapped trace chunks. We then report selected experimental
results to validate our expectations. We Show that it is possible to achieve near-perfect speed-up without loss of
accuracy. Next, in order to achieve further reduction in simulation cost, we combine uniform **sampling** methods with
parallel trace processing with a slight loss of accuracy for finite-cache timer runs. We then show that by using warm-start
sequences...

29/3,K/3 (Item 1 from file: 35) <u>Links</u>
Dissertation Abs Online
01518793 ORDER NO: AAD96-35606
GOAL-DIRECTED PERFORMANCE TUNING FOR SCIENTIFIC APPLICATIONS (COMPILERS)
Author: SHIH, TIEN-PAO
Degree: PH.D.
Year: 1996
Corporate Source/Institution: THE UNIVERSITY OF MICHIGAN (0127)
Source: Volume 5707B of Dissertations Abstracts International.
PAGE 4526 . 158 PAGES
   ...objective. A case study shows an average 1.79x speedup achieved by using this approach for the Livermore Fortran
Kernels 1-12 running on the **IBM** RS/6000.
   For memory, as compulsory and capacity misses are relatively easy to characterize, we derive a method for building
application-specific cache behavior **models** that report the number of misses for all three types of conflict misses: self,
cross, and ping-pong. The method uses averaging concepts to determine the expected number of **cache misses** instead

of attempting to count them exactly in each instance, which provides a more rapid, yet realistic assessment of expected cache behavior. For each type... ...data layout: array padding, initial address adjustment, and access resequencing. A case study using a blocked matrix multiply program as an example shows that the **model** is within 11% of the simulation results, and that each type of conflict miss can be effectively reduced or completely eliminated.

For communication in shared...

29/3,K/4 (Item 2 from file: 35) <u>Links</u>
Dissertation Abs Online
(c) 2007 ProQuest Info&Learning. All rights reserved.
01379842 ORDER NO: NOT AVAILABLE FROM UNIVERSITY MICROFILMS INT'L.
PERFORMANCE IMPACT OF SHARED MEMORY LATENCY IN MULTIPROCESSORS: MODELS AND EXPERIMENTS
Author: BRORSSON, MATS
Degree: TEKN.DR
Year: 1994
Corporate Source/Institution: LUNDS UNIVERSITET (SWEDEN) (0899)
Source: Volume 5504C of Dissertations Abstracts International.
PAGE 1264 . 20 PAGES
Location of Reference Copy: DEPARTMENT OF COMPUTER ENGINEERING, LUND UNIVERSITY, P.O. BOX 118, S-221 00 LUND, SWEDEN
...techniques are presented. An analytic model of single-program-multiple-data program execution time has been used to explain the execution time measurements on the **IBM** RP3 experimental multiprocessor. The model is shown to be useful to predict execution times divided in serial section, parallel section and linear contention execution times... ...such as execution-driven simulation.

The second section considers the impact of the access pattern to shared data on the shared memory latency. A visual **model** of the shared data access pattern has been developed to qualitatively compare the performance of parallel applications for a given architecture. Examples are given that demonstrate that performance bottlenecks are easily spotted with the visual **model**.

The visual **model** has been refined in order to quantitatively predict the number of **cache misses** for different access categories. Architectural simulations have been used to verify the accuracy of the quantitative **model**. The number of cold, coherence and directory replacement misses for write-invalidate, directory-based cache coherence protocols can be predicted with high accuracy for three...

29/3,K/5 (Item 1 from file: 2) <u>Links</u>
INSPEC
(c) 2007 Institution of Electrical Engineers. All rights reserved.
06376112 **INSPEC Abstract Number:** C9610-5470-027
Title: A three-parameter fast Givens QR algorithm for superscalar processors
Author Carrig, J.J., Jr.; Meyer, G.G.L.
Author Affiliation: Dept. of Electr. & Comput. Eng., Johns Hopkins Univ., Baltimore, MD, USA
Conference Title: Proceedings of the 1996 International Conference on Parallel Processing. Vol.2 Algorithms and Applications   **Part** vol.2   p. 11-18 vol.2
Editor(s): Bojanczyk, A.
Publisher: IEEE Comput. Soc. Press , Los Alamitos, CA, USA
Publication Date: 1996 **Country of Publication:** USA   3 vol. (xvi+278+xv+173+230) pp.
ISBN: 0 8186 7623 X   **Material Identity Number:** XX96-02685
U.S. Copyright Clearance Center Code: 0190-3918/96/$5.00
Conference Title: Proceedings of 25th International Conference on Parallel Processing
Conference Sponsor: Int. Assoc. Comput. & Commun.; Pennsylvania State Univ
Conference Date: 12-16 Aug. 1996   **Conference Location:** Ithaca, NY, USA
Language: English
 Subfile: C
 Copyright 1996, IEE
Abstract: ...a selection of parameter values for which the new algorithm reduces to the standard algorithm, but show that non-standard values minimize the number of **cache misses**, memory references and pipeline stalls. Using a tractable **model** of a superscalar machine architecture, we derive rules for estimating the optimal combination of parameter values. Applying these rules, we observe a speedup over the standard algorithm of 2.4 on the Intel Pentium Pro system, 2.0 on a single thin POWER2 processor of the **IBM** SP2, 1.6 on a single wide POWER2 processor of the **IBM** SP2, and 4.2 on a single R8000 processor of the SGI POWER Challenge XL.
Identifiers: ...**IBM** SP2

29/3,K/6 (Item 2 from file: 2) <u>Links</u>
 Fulltext available through: <u>ACM - Association for Computing Machinery</u> <u>USPTO Full Text Retrieval Options</u>
INSPEC
(c) 2007 Institution of Electrical Engineers. All rights reserved.
06276714 **INSPEC Abstract Number:** C9607-6150J-014
Title: The measured performance of personal computer operating systems
Author Chen, J.B.; Endo, Y.; Kee Chan; Mazieres, D.; Dias, A.; Seltzer, M.; Smith, M.D.
Author Affiliation: Div. of Appl. Sci., Harvard Univ., Cambridge, MA, USA
Journal: ACM Transactions on Computer Systems   vol.14, no.1   p. 3-40

Abstract: The article presents a comparative study of the performance of three operating systems that run on the personal computer architecture derived from the IBM PC. The operating systems, Windows for Workgroups, Windows NT, and NetBSD (a freely available variant of the Unix operating system), cover a broad range of system functionality and user requirements, from a single address space model to full protection with preemptive multitasking. Our measurements are enabled by hardware counters in Intel's Pentium processor that permit measurement of a broad range of processor events including instruction counts and on chip cache miss counts. We use both microbenchmarks, which expose specific differences between the systems, and application workloads, which provide an indication of expected end to end performance...
Descriptors: IBM computers...
 Identifiers: ...IBM PC

 29/3,K/7 (Item 3 from file: 2) Links
INSPEC
05112726   INSPEC Abstract Number: C9204-5420-003
Title: IBM 3090 memory access; measurement and simulation
Author Homberg, W.; Hake, J.-Fr.; Gurich, W.
Author Affiliation: Forschungszentrum Julich GmbH, Germany
Conference Title: Proceedings SHARE Europe Spring Meeting. CASE and Applications Development in Practice   p. 353-8
Publisher: SHARE Europe , Geneva, Switzerland
Publication Date: 1991 Country of Publication: Switzerland   488 pp.
Conference Date: 8-12 April 1991   Conference Location: Lausanne, Switzerland
Language: English
 Subfile: C
Title: IBM 3090 memory access; measurement and simulation
Abstract: ...traffic. Different architectural concepts are provided to diminish this effect. One attempt to reach this goal is the implementation of a hierarchical memory structure. On IBM computers, this hierarchy includes CPU, cache (high-speed buffer), main memory, and paging devices (e.g. expanded storage and disks). A model is developed focusing on the memory architecture of the IBM 3090 family. In particular, the behavior of sequential algorithms with respect to cache and translation lookaside buffer (TLB) is considered. For a given sequence of memory references the numbers of cache misses and TLB misses are calculated and the amount of CPU time consumed by these effects can be estimated. Parameters describing the buffer size, line length, the number of sets, and different replacement algorithms are taken into account. The model is verified by studying the performance of application-oriented programs from numerical linear algebra with a known memory access pattern. Jobs were run on IBM 3090 computers differing in cache size and processor cycle time at KFA Julich (IBM 3090 200E) and RWTH Aachen (IBM 3090 600S). The measured CPU time consumption is compared with the predicted results showing that measurement and simulation are in good agreement.
Descriptors: ...IBM computers
Identifiers: ...IBM computers... ...IBM 3090

 29/3,K/8 (Item 1 from file: 256) Links
TecInfoSource
00152923   Document Type: Review
Product Names: Apple G5 (221777); Opteron (146731); Athlon (169137); 64-bit Computing (810801)
Title: Faster, More Powerful...64 bits!
Author: Asaravala, Amit
Source: Software Development ;   v12 n4 p28(5) Apr 2004
ISSN: 1070-8588
Homepage: http://www.sdmagazine.com
File Segment: Review
Record Type: Product Analysis
Revision Date: 20070300
Apple Computer's G5, IBM's PowerPC 970, and AMD's Opteron and Athlon are among highlighted faster, more powerful 64-bit processors. To gain the advantages of 64-bit... ...64-bit processor, in great part because 64-bit addresses take up more space in the cache than 32-bit addresses, which means a higher cache miss rate. Wider registers do allow larger numbers to be stored concurrently, and 64-bit processors eliminate the need to use two registers for many large... ...in the world, and was designed to run some of the most bleeding edge applications in nanoscale electronics, chemistry/biochemistry, aerodynamics, molecular statics, cell cycle modeling, and computational acoustics. Also

described are other features that make 64-bit processors faster, including the AMD x84-64 ISA's 16 (8 more than...

29/3,K/9 (Item 1 from file: 239) <u>Links</u>
Mathsci
(c) 2007 American Mathematical Society. All rights reserved.
03518382 **MR** 2004d#65002
Tenth SIAM Conference on Parallel Processing for Scientific Computing.
Proceedings of the conference held in Portsmouth, VA, March 12--14, 2001. Edited by Charles Koelbel, Juan Meza et al.
Contributors: Koelbel, Charles; Meza, Juan; et al.
Publisher: Society for Industrial and Applied Mathematics (SIAM), Philadelphia, PA,
  2001 , 1 CD-ROM (Windows, Macintosh and UNIX). **ISBN:** 0-89871-492-3
Language: English
Conference: Parallel Processing for Scientific Computing,; Portsmouth, VA,   10th SIAM 2001
Subfile: MR (Mathematical Reviews) AMS
Abstract Length: LONG (165 lines)
Reviewer: Editors
...Uintah PSE (8 pp.); Rob F. Van der Wijngaart and Michael Frumkin, Interference lattice-based loop nest tilings for stencil computations (11 pp.); Somnath Ghosh, **Cache miss equations**: compiler analysis framework for tuning memory behavior (11 pp.); Michael Frumkin and Rob F. Van der Wijngaart, Using minimum-surface bodies for iteration space partitioning... ...support for adaptive computation (12 pp.); A. A. Mirin, R. H. Cohen, B. C. Curtis, et al., Accomplishing very high resolution turbulence simulations on the **IBM**-SP system (9 pp.).
 William F. Mitchell, A refinement-tree based partitioning method for adaptively refined grids (11 pp.); Robert Oehmke and Quentin F. Stout... ...affine partitioning (13 pp.); Rupak Biswas and Leonid Oliker, Ordering sparse matrices for cache-based systems (3 pp.); Hongli Zhang and Margaret Martonosi, A mathematical **cache miss** analysis for pointer data structures (11 pp.); Jens Mache, Joshua Bower-Cooley, Robert Broadhurst, Jennifer Cranfill and Clark Kirkman, IV, Parallel I/O performance of PC clusters (10 pp.); Xing Cai and Asmund Odegard, On the performance of PC clusters in solving partial differential **equations** (10 pp.); W. Rivera, J. Zhu and D. H. Huddleston, Parallel performance investigation of a domain decomposition algorithm (10 pp.); Chialin Chang, Tahsin Kurc, Alan...

Set	Items	Description
S1	2550966	(IBM OR INTERNATIONAL()BUSINESS()MACHINE? OR IBM()CORP OR IBM()CORPORATION OR BIG()BLUE)
S2	54235	(MEMORY OR RAM? ? OR ROM? ? OR PROM? ? OR EPROM? ? OR EEPROM? ? OR DRAM? ? OR SDRAM? ? OR RDRAM? ? OR DIMM? ? OR SODIMM? ? OR ECC OR SIMM OR (DATA OR CACHE)(1W)(STORE OR ORAGE) OR READ()ONLY OR READ(1N)WRITE)(5N)(OPTIMI?ATION OR
S3	242	CACHE(1W)MISS??(5N)(REDUCE OR LIMIT? OR LIMITATION? ? OR NSTRAIN OR RESTRICT??? OR RESTRICTION? ? OR LOWER??? OR SSEN??? OR MITIGAT??? OR MODERAT??? OR NEGATE? ? OR NEGAT??? MINIMI?)
S4	0	S2(10N)S3
S5	0	S4(5N)(PROFIL??? OR INSTRUMENTATION OR CHARACTERIZATION OR MMARY OR SURVEY OR CHART OR INTERPRETATION)
S6	10104	S S1 AND S2
S7	3966	S S1(100N)S2
S8	4	S S1 AND (S2(100N)(CACHE(1W)MISS))
S9	4	S S8 NOT PY=2003:2007
S10	2	RD (unique items)
S11	85	S S3 AND S1
S12	145	S S1 AND (S2(20N)(PROFIL??? OR INSTRUMENTATION OR CHARACTERIZATION OR SUMMARY OR SURVEY OR CHART OR INTERPRETATION))
S13	1039	S S1 AND (S2(20N)(STATISTIC?? OR HEURISTIC? ? OR LOGARITHM?? OR WEIGHT??? OR MODEL??? OR MODEL??? OR METRICS OR FORMULA? ? OR SUM? ? OR EQUATION? ? OR QUANTITATIVE()ANALYSIS OR SAMPL??? OR ANALYTICAL))
S14	64	S S11 NOT PY=2003:2007
S15	44	RD (unique items)
S16	44	SORT S15/ALL/PY
S17	41	S S1 (100N)(S2(10N)(PROFIL??? OR INSTRUMENTATION OR CHARACTERIZATION OR SUMMARY OR SURVEY OR CHART OR INTERPRETATION))
S18	214	S S1 (100N)(S2(5N)(STATISTIC?? OR HEURISTIC? ? OR LOGARITHM?? OR WEIGHT??? OR MODEL??? OR MODEL??? OR METRICS OR FORMULA? ? OR SUM? ? OR EQUATION? ? OR QUANTITATIVE()ANALYSIS OR SAMPL??? OR ANALYTICAL))
S19	35	S S17 NOT PY=2003:2007
S20	17	RD (unique items)
S21	210	S S18 NOT (S19 OR S14 OR S8)
S22	122	RD (unique items)
S23	116	S S22 NOT PY=2003:2007
S24	158	S S1 (50N)(S2(5N)(STATISTIC?? OR HEURISTIC? ? OR LOGARITHM?? OR WEIGHT??? OR MODEL??? OR MODEL??? OR METRICS OR FORMULA? ? OR SUM? ? OR EQUATION? ? OR QUANTITATIVE()ANALYSIS OR SAMPL??? OR ANALYTICAL))
S25	157	S S24 NOT (S19 OR S14 OR S8)
S26	90	RD (unique items)
S27	86	S S26 NOT PY=2003:2007
S28	83	S S1 (20N)(S2(5N)(STATISTIC?? OR HEURISTIC? ? OR LOGARITHM?? OR WEIGHT??? OR MODEL??? OR MODEL??? OR METRICS OR FORMULA? ? OR SUM? ? OR EQUATION? ? OR QUANTITATIVE()ANALYSIS OR SAMPL??? OR ANALYTICAL))
S29	82	S S28 NOT (S19 OR S14 OR S8)
S30	76	S S29 NOT PY=2003:2007
S31	50	RD (unique items)S

[File 15] **ABI/Inform(R)** 1971-2007/Mar 19
[File 9] **Business & Industry(R)** Jul/1994-2007/Mar 16
[File 635] **Business Dateline(R)** 1985-2007/Mar 17
[File 610] **Business Wire** 1999-2007/Mar 19
[File 810] **Business Wire** 1986-1999/Feb 28
[File 647] **CMP Computer Fulltext** 1988-2007/May W4
[File 674] **Computer News Fulltext** 1989-2006/Sep W1
[File 20] **Dialog Global Reporter** 1997-2007/Mar 19
[File 275] **Gale Group Computer DB(TM)** 1983-2007/Mar 16
[File 621] **Gale Group New Prod.Annou.(R)** 1985-2007/Mar 08
[File 47] **Gale Group Magazine DB(TM)** 1959-2007/Mar 08
[File 636] **Gale Group Newsletter DB(TM)** 1987-2007/Mar 16
[File 148] **Gale Group Trade & Industry DB** 1976-2007/Mar 08
[File 16] **Gale Group PROMT(R)** 1990-2007/Mar 16
[File 484] **Periodical Abs Plustext** 1986-2007/Feb W4
[File 813] **PR Newswire** 1987-1999/Apr 30
[File 613] **PR Newswire** 1999-2007/Mar 19
[File 634] **San Jose Mercury** Jun 1985-2007/Mar 16
[File 553] **Wilson Bus. Abs.** 1982-2007/Mar
[File 98] **General Sci Abs** 1984-2007/Mar
[File 88] **Gale Group Business A.R.T.S.** 1976-2007/Mar 14
[File 996] **NewsRoom 2000-2001**
[File 993] **NewsRoom 2004** (c) 2006 Dialog
[File 995] **NewsRoom 2002**
[File 992] **NewsRoom 2005**

Higher relevance

d

Subject summary

10/3,K/1 (Item 1 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01256152   Supplier Number: 06615136 (Use Format 7 Or 9 For FULL TEXT)
IBM PS-2 Model 70-A21. (Hardware Review) (evaluation)
PC Tech Journal , v6 , n9 , p76(2)
Sept , 1988
Document Type: evaluation
ISSN: 0738-0194
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 1289   Line Count: 00096
IBM PS-2 Model 70-A21. (Hardware Review) (evaluation)

Abstract: IBM's PS-2 Model 70-A21 is a 386-based microcomputer with 32-bit memory (expandable to 16Mbytes),
an ESDI hard disk, and an optional...

Unlike the ALR, Compaq, and Everex products, which are refinements of
existing models, the IBM Model 70-A21 is a wholly new system.
Announced 14 months after the April 2, 1987, introduction of the PS/2
series of computers, the A21 is one of three new desktop 386 systems that
IBM hopes will carve out a substantial share of the 386 market,
which Compaq now dominates.
      The Model 70 series includes the 16-MHz entry-level...
...of 1988. The A21 reviewed was examined and tested prior to general
availability. Assuming the production A21 performs as well as the review
unit, then IBM uncharacteristically has produced a very
high-performance computer.
      The Model 70s are nearly identical in appearance to the Model 50 and
the new zero-wait...
...features are the extra ventilation slots on the right side of the
system-unit cover and the Model 70 386 label on the oval-shaped IBM
PS/2 logo. INSIDE THE BOX The Model 70 bears a resemblance to the Model 50
on the inside as well. The interior contains no...
...printed circuit board. The Model 70 supports a single hard-disk drive
(the 120MB unit, with its integrated ESDI, is the only one offered by
IBM).
      One 3.5-inch, 1.44MB diskette drive is standard on the Model 70; a
second 1.44MB diskette drive and an external 5.25...
...the optional 387 math coprocessor are mounted on a daughterboard
attached to the system board. The daughterboard attaches with two
2-by-40-pin connectors.
      IBM's creative use of the 82385 allows it to control a two-way
associative 64KB memory cache, rather than the 32KB cache used on the...
...cache miss and a memory-page miss occur. Memory writes are buffered
outside the CPU and occur at zero wait states as long as a cache
miss or other memory-write operation does not occur before the
current write operation completes.
      The user can add memory to the Model 70 using a...
...can be used, with no switch setting required. The board requires a
32-bit Micro Channel slot; multiple boards can be installed to provide a
maximum 16MB of system memory. The memory-expansion
board can be used on the PS/2 Model 80 as well as the Model 70.
      IBM's ability to put a large amount of logic into a small
space is apparent in the A21 system board. With extensive use of
surface-mount technology and efficient use of the vertical and horizontal
space, IBM made the system board small enough to fit into the small
footprint of the Model 50. Several components, including the SIMMs and the
VGA video...
...device shelf above them. All vertically mounted components are firmly
attached to the system board and should not hinder the reliable operation
of the system; IBM and its dealers, however, will have to take extra
care to ensure that these parts are not damaged during shipping.
      The Model 70 features the...
...VGA used on previous models, unfortunately still with an 8-bit
interface. Apparently, higher-performance video will not be standard on a
PS/2 until IBM decides to integrate 8514/A-type capabilities onto
the system board.
      Like other PS/2s, the Model 70 system board holds the VGA, serial,
parallel, mouse, and keyboard ports. IBM has added coils to Model 70
ports to help control electrical emissions.

The Model 70 system board has three Micro Channel slots--one 16-bit

...

...any matched memory-cycle requests from the board. PERTINENT PAPERS Like
all PS/2s, the Model 70 is well documented. The quick-reference guide
provides IBM's usual pictorial and verbal explanations of setup,
installation of options, and ...for "no" or "not" (a circle with a slash
through it) superimposed over the letters "OK" and an arrow pointing to a
representation of an IBM manual, the message means "the system is
not okay, consult the manual." The quick-reference guide offers the
simplistic advice that the system unit should...
...after booting the system using the Reference Diskette.
Technical information on the Model 70 and its various submodels is
available at extra cost in the IBM PS/2 Hardware Interface Technical
Reference. This manual, intended for developers of PS/2 hardware and
software products, provides information on the Micro Channel architecture
and the PS/2 Models 50, 60, 70, and 80. BIOS information is available in
the IBM Personal System/2 and Personal Computer BIOS Interface
Technical Reference.
IBM provides technical information on the 120MB hard disk and
2-8MB 80386 memory-expansion option in separate technical references.
Maintenance information is provided on supplements...
Captions:

IBM PS-2 Model 70-A21 vital statistics. (table)
Company Names:
International Business Machines Corp...
Trade Names:
IBM PS/2 70 A21 (Microcomputer...

10/3,K/2 (Item 2 from file: 275) Links
Gale Group Computer DB(TM)
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01208687   Supplier Number: 05107119 (Use Format 7 Or 9 For FULL TEXT)
Speed infusion: part 3. (11 accelerator boards for IBM PCs and compatibles) (Hardware Review) (evaluation)
Mirecki, Ted
PC Tech Journal , v5 , n6 , p118(12)
June , 1987
Document Type: evaluation
ISSN: 0738-0194
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 2775   Line Count: 00205
Abstract: The three classes of accelerator boards for IBM PCs and compatibles are Class I, which provide faster clock
rates; Class II, which replace the 8088 microprocessor with an 8086; and Class III, which...

16/3,K/1 (Item 1 from file: 88) <u>Links</u>
Gale Group Business A.R.T.S.
02067262   **Supplier Number:** 06276170
The search for performance in scientific processors. (Turing Award lecture)
Cocke, John
Communications of the ACM , v31 , n3 , p250(4)
March , 1988
ISSN: 0001-0782
Language: English   **Record Type:** Fulltext; Abstract
Word Count: 2780   **Line Count:** 00277
...projects that I have participated in. They were interesting because I
felt I learned faster during these projects than at other times.
    When I joined **IBM** in 1956, the Stretch project was underway.
The project was led by Steve Dunwell, who placed performance, not cost, as
paramount. My experience had consisted...general purpose problems.
    These are only a few of the features we had in ACS. Many ideas have
found their way into subsequent machines at **IBM** particularly in the
cache area. Some of the more intricate ones, however, have not yet been
used. In many cases this was due to cost...by others and stimulated
considerable additional research and experimentation in many universities.
Berkeley coined the name "RISC" (Reduced Instruction Set Computing) for
similar work.
    Within **IBM** we feel it is extremely important to simulate the
hardware of a new machine extensively. As the complexity of machines
increased, the time required to...
...us to use the machines only for long-running simulations. In spite of
this time-consuming difficulty, many such machines are in constant use at
IBM. The next generation logic simulator, with added switching
capacity, is being built to ease this problem.
    Note; however, that the nonblocking switches grow at least...
...challenges will lie in compiler optimization techniques, both to
recognize the parallelism and schedule the instructions. O ne particularly
difficult yet crucial problem is to **minimize cache
misses** in these parallel processors. For example, on an inner loop
that goes at three instructions per cycle on a machine that has a cache
taking...

 16/3,K/2 (Item 2 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
01251739   **Supplier Number:** 06833881 **(Use Format 7 Or 9 For** FULL TEXT)
Cache controllers flare memory bottleneck. (includes related article)
Leonard, Milt; Bursky, Dave
Electronic Design , v36 , n8 , p25(6)
March 31 , 1988
ISSN: 0013-4872
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 2189   **Line Count:** 00166

...associative cache with LRU and write-buffering features (Fig. 2). Memory
hit statistics gathered by Austek show that a four-way set-associative
cache can **reduce** the number of **cache misses** by 25%
over a two-way set associative cache and by 40% over a direct-mapped cache.
    Like the Intel controller, the 38152 employs bus...controller.
Moreover, Austek is the only company with an alternate source for its
controller: Zymos, a company well known for its cluster chips sold to
IBM PC-clone manufacturers. Zymos, however, will offer the 38152
only as part of its motherboard chip sets.
    Another new cache controller the NS32605, is made...

 16/3,K/3 (Item 3 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
01236820   **Supplier Number:** 06458065 **(Use Format 7 Or 9 For** FULL TEXT)
**Novel DSP boards break through speed bottlenecks. (digital signal processing, includes related articles on bus
transfer rates, filters, and measuring DSP performance data) (Electronic Design Report)**
Phillips, Barry W.
Electronic Design , v36 , n4 , p132(13)
Feb 18 , 1988

ISSN: 0013-4872
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 4538   **Line Count:** 00344

...manipulation or Spice calculations.
    In fact, many designers are doing just that with cards plugging into
a personal computer. For one thing, an 80286-based **IBM PC AT**,
executing half a million instructions per second--even with its 100-kFLOPS
80287 coprocessor--runs out of steam when tackling simulation programs that
...at any one time is small compared with cache size, the processor
typically crunches along without having to wait for fetches to main memory.
To **reduce cache miss** overhead, when instructions that
don't reside in the cache are requested, the MC3200 processor fetches the
next 16 instructions rather than just the next...

  16/3,K/4 (Item 4 from file: 275) **Links**
Gale Group Computer DB(TM)
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01319755   **Supplier Number: 07993470 (Use Format 7 Or 9 For** FULL TEXT)
Compilers unlock RISC secrets. (compiler optimization key to RISC performance potential) (reduced-instruction-set computers; includes a related article on optimization to improve cache performance)
Weber, Larry B.
ESD: The Electronic System Design Magazine , v19 , n12 , p26(5)
Dec , 1989
ISSN: 0893-2565
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 3289   **Line Count:** 00272

...miss less frequently than data references; this observation allows the
compiler to prefer slightly longer instruction sequences if they avoid
extra data references. The instruction **cache miss** rate is
lower because the hardware loads multiple contiguous words into the
cache on a miss, and the sequential nature of instruction execution takes
advantage of this locality...make them compatible with other
implementations. An important set of extensions is the support of the DEC
VMS Fortran extensions. Another is the inclusion of **IBM PL1**
extensions to permit an independent software vendor to port a
1.8-million-line PL1 program to the MIPS architecture.
    Wherever extensions are required...C, with the added capacity of data
abstraction. (See p. 35, this issue.)
    It is expected that future compilers will take advantage of
optimizations that **reduce cache misses**. These
optimizations include loop interchange, which reorders the accesses to an
array to improve locality of data references, and software pipelining,
which takes better advantage...

  16/3,K/5 (Item 5 from file: 275) **Links**
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01295886   **Supplier Number: 07584593 (Use Format 7 Or 9 For** FULL TEXT)
Profiles in learning. (examples of neural network simulations)
Passarelli, Ben
UNIX Review , v7 , n5 , p50(6)
May , 1989
ISSN: 0742-3136
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 2414, **Line Count:** 00204

...the inherent parallelism of neural algorithms. To perform this work,
they have developed a parallel processing system using Inmos T-800
transputers connected to an **IBM** PC AT host. A transputer is a
specialized coprocessor capable of pipelined arithmetic operations that can
be easily configured to route data arbitrarily to other...neural-network
algorithms. Fully interconnected neural networks, for example, place
tremendous demands on distributed or cached memory architectures. Such
systems generally require algorithm restructuring to **reduce**
interprocessor communication or **cache misses** before they can
attain optimal performance.
    Furthermore, the degree of network connectivity determines the
optimal performance achievable using a particular processor type. Fully

interconnected or...

16/3,K/6 (Item 6 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01288597   Supplier Number: 07060390 (Use Format 7 Or 9 For FULL TEXT)
The Clipper (TM) Processor: instruction set architectures and implementation. (product announcement)
(technical)
Hollingsworth, Walter; Sachs, Howard; Smith, Alan Jay
Communications of the ACM , v32 , n2 , p200(20)
Feb , 1989
Document Type: technical
ISSN: 0001-0782
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 9556   **Line Count:** 00758

...processor are in high performance workstations and "super-minicomputer"
shared machines. To introduce some historical perspective, the highest
performance commercial mainframe in 1976 was the IBM 370/168, which
for the kind of workloads expected on CLIPPER (C, Fortran, Pascal), had
performance comparable to that of the C100 CLIPPER.
    When the...
...architectures, shifted in the 1980s toward very simple architectures, as
originally implemented in the Cray machines (CDC 6400, 6600, 7600), studied
and implemented in the IBM 801, and further studied and popularized
by the RISC project at Berkeley and the MIPS project at Stanford. The
essence of such machines is a...also facilitates upgrading low performance
(big-endian) machines with higher performance, CLIPPER-based products. (In
contrast, when data is exchanged between a Vax and an IBM 370, bytes
must be explicitly swapped.)
    Data Types
    The selection of data types represents a compromise between apparent
functionality, which is enhanced by a large...only those registers that
have been modified, and passes the first two arguments in registers. For
comparison, we note that both the Vax and the IBM 370 have 16 GPRs.
Lunde's results suggest that 8 to 10 registers are almost always
sufficient. Analyses in show that with intra-procedure register...
...of eight double precision floating point (FP) registers accessible
inboth user and supervisor states; floating point instructions refer to
these. This is similar to the IBM 370 design, in which there are
four FP registers. Eight registers provide sufficient storage for temporary
operands, whereas four are insufficient in the absence of...
...microprocessor has a load/store architecture; i.e., most of the
references to memory are via load and store instructions in contrast to
both the IBM 370 and DEC Vax which make extensive use of their
register/memory operations (370 RX ...as the Vax, the National 32000 and
the Intel 80386, but provides considerably denser code than RISC processors
such as the SUN Sparc and the IBM ROMP. (CLIPPER does have some SS
operations implemented in the MIROM.) For RISC-I [32], a 2/3 increase in
number of instructions over the...
...closely correlated. There are two advantages to small code sizes: there
is less memory traffic, which is a limiting factor in most multiprocessor
designs, and **cache miss** ratios are **lower**, since
working sets are smaller; see [14] for analyses and comparative miss
ratios.
    For load and store instructions, CLIPPER provide nine addressing
modes, which appear...
...with 32-bit displacement) is very useful. The long 32-bit displacement
eliminates the aggravating addressability problem posed by the 12-bit
displacement of the IBM 370. The register + 12-bit displacement mode
saves 4 bytes, if only a short displacement is needed, and the relative
(register with no displacement) mode...
...the 16-bit form, for references to low memory and within small programs.
    A PC-relative address mode would have been very useful in the
IBM 370 [35], and such modes are provided by CLIPPER. The PC can be
used with 16- or 32-bit displacement or with a register (GPR...condition
codes, which are set by one instruction and read and used by a subsequent
instruction; this is similar to what is done on the IBM 370. Using
condition codes for branching yields better performance and less complexity
than an instruction that both tests and branches.

Four standard condition codes--N is released, use the wait
instruction to sleep, or task switch. Test and set is also used by the
IBM 370 and the M68000; the Vax provides seven instructions for
locking and synchronization, some of which are equivalent to test and set.
Test and set...Vax has a CISC instruction set, and thus generally runs at
about 0.5 MIPS. The Vax 11/780 runs about as fast as an IBM
System/370 machine running at 1 MIPS on a scientific workload.)
    While there is considerable variation among the various benchmarks,
the C100 CLIPPER is approximately...

16/3,K/7 (Item 7 from file: 275) Links
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01389549   Supplier Number: 09846549 (Use Format 7 Or 9 For FULL TEXT)
Register windows speed real-time control tasks.
Bursky, Dave
Electronic Design , v38 , n21 , p57(4)
Nov 8 , 1990
ISSN: 0013-4872
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 2293   Line Count: 00181
...It also contains another eight programmable chip-select lines that
simplify the attachment of off-chip, low-cost DRAMs.
    Special page-mode detection logic helps minimize the
cache-miss penalty. Each time there's a cache miss, a
worst-case assumption is that the first word accessed is in a new memory
page. That of those tools include native (Sun-4) and cross tools (Sun-3 and
IBM PC and compatibles)-C compilers, linkers, loaders, librarian,
libraries, target monitor, and so on.
    For additional software, Fujitsu struck a deal with Microtec Research
Inc...

16/3,K/8 (Item 8 from file: 275) Links
Gale Group Computer DB(TM)
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01372858   Supplier Number: 08752644 (Use Format 7 Or 9 For FULL TEXT)
Cache considerations for multiprocessor programmers. (cache memory) (technical)
Hill, Mark D.; Larus, James R.
Communications of the ACM , v33 , n8 , p97(6)
August , 1990
Document Type: technical
ISSN: 0001-0782
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 2736   Line Count: 00223

...surrounding the most recent memory references. Finite caches limit
locality on both uniprocessors and multiprocessors.
    In the uniprocessors, limited chaches are the principal cause of
cache misses. To reduce the number of misses, data
should be organized with common access patterns referencing adjacent words;
this enables the cache to hold the last C- referenced...Vitual Memory
Systems. ACM Trans. Comput. Syst. 7, 4 (November 1989), 321-359.
    [10] Liu, B. and Strother, N. Programming in VS Fortran on the
IBM 3090 for Maximum Vector Performance. IEEE Computer, 21, 6 (June
1988), 65-76.
    [11] Rudolph, L. and Segall, Dynamic Decentralized Cache Schemes for
MIMD Parallel...

16/3,K/9 (Item 9 from file: 275) Links
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01344561   Supplier Number: 08022142 (Use Format 7 Or 9 For FULL TEXT)
Northgate to price powerful 486 PC at under $10,000. (Northgate Computer Systems Inc.)
Grossman, Evan O.
PC Week , v6 , n1 , p1(8)
Jan 8 , 1990
ISSN: 0740-1604
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 385   Line Count: 00030

...the first 486 systems to feature an AT bus coupled with external 486
cache memory and burst-mode operation, according to company officials.
     Burst mode "minimizes the penalty of a cache
miss," said Eshok Bansel, a product manager at Chips &
Technologies Inc., the San Jose, Calif., chip maker. Burst mode is twice as
fast as conventional memory...
...The system will cost between $8,000 and $10,000, said Graham Beachum
Jr., executive vice president of Northgate in Plymouth, Minn.
     Although companies including **IBM**, AST Research Inc. and Everex
Systems Inc. have announced 486-based systems, those products are based on
daughtercard implementations that do not include external cache...
Trade Names:
...**IBM** PC AT (Microcomputer

 16/3,K/10 (Item 10 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01452993   Supplier Number: 11330383 **(Use Format 7 Or 9 For** FULL TEXT **)**
Power platform; shopping for a 486. (Buying) (Intel 80486-based microcomputers) (includes related guide to component prices) (tutorial)
Rowell, Dave
PC Sources , v2 , n10 , p206(12)
Oct , 1991
Document Type: tutorial
ISSN: 1052-6579
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 7865   **Line Count:** 00577

...main memory design and DRAM chip speed. Most 486 systems use interleaved
memory, page-mode memory, or a combination of the two memory architectures
to **reduce** wait states during **cache misses**, those times
when the cache fails and the cache controller must read from the DRAMs in
main memory. The higher the clock speed, the more...
...486 motherboard require four SIMMs or 36 DIP chips. With interleaving,
you must double those numbers, adding SIMMs in groups of eight. Faster
DRAMs also **reduce** wait states during **cache misses**.
Most 486/25 PCs use chips with 80ns or lower access times, while 33MHz
systems are better off with 70ns or faster memory chips.
     In...bus is the biggest bottleneck on a large file server for both
the hard drives and the network adapter card.
     To remove the bus bottleneck, **IBM** developed the Micro Channel
Architecture (MCA) bus found on its faster PS/2 PCs and now also on Micro
Channel clones. In response, the manufactuers of **IBM**-compatible PCs
developed the competing Extended Industry Standard Architecture (EISA)
expansions bus. By default, the old AT-compatible bus found on most PCs
becomes Industry...

 16/3,K/11 (Item 11 from file: 647) <u>Links</u>
CMP Computer Fulltext
(c) 2007 CMP Media, LLC. All rights reserved.
00602235 **CMP Accession Number:** UNX19910415S1826
HP's Powerful New PA-RISC Chip - New Architecture Gives Latest HP Box Impressive Performance Gains At A Low Cost
ROBERT B.K. DEWAR ; MATTHEW SMOSNA
UNIX TODAY , 1991 , n 069 , 44
Publication Date: 910415
Journal Code: UNX **Language:** English
Record Type: Fulltext
Section Heading: technology
Word Count: 1663
Text:

...of the scale, Sun's SPARCstation SLC is inexpensive but has limited
performance, particularly in floating- point applications. At the other end
of the scale, IBM's high-end RS/ 6000 offers very high performance,
but at a price.

...to load the contents of the rest of the line from memory into the
cache. The architecture also has interlocks, so the penalty of a

cache miss (when it does happen) is **minimized.**
    The combination of these approaches means that the PA-RISC 1.1 can
achieve very impressive performance without the added complication of
superscalar and superpipelined...

16/3,K/12 (Item 12 from file: 148) <u>Links</u>
Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rights reserved.
05578681   **Supplier Number:** 11716494 (USE FORMAT 7 OR 9 FOR FULL TEXT)
EDN Special Report: 32-bit floating-point DSP processors. (digital signal processing) (Cover Story)
Weiss, Ray
EDN , v36 , n23 , p126(15)
Nov 7 , 1991
Document Type: Cover Story
ISSN: 0012-7515
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 6888   **Line Count:** 00574

...multimedia processing. And the software is falling into place to ease
the transition from microprocessorto DSP-style processing. "Programming DSP
chips," says Jimmie Edrington, an **IBM** design engineer, "is no more
difficult to learn than programming a microprocessor."
    However, dedicated DSP processors are not alone. Standard RISC
processors are taking on...cases, limited multiprocessing is all that's
needed for dedicated applications such as graphics and image processing.
For example, the new graphics subsystem for the **IBM** RS/6000
workstations is based on multiple TMS320C30s. The subsystem can do
highresolution 2- and 3-D graphics on an X terminal. "We've looked at the
C40, and it looks good, but we just don't need the communications
capability for our application," says **IBM**'s Jimmie Edrington. "In
fact, I wish TI would move some of the instruction upgrades in the C40 back
into the C30 where we could...still rely on assembly language for fast,
critical code, such as for algorithm inner loops. "I do about 90% of my
code in C," says **IBM**'s Edrington, "and 10% in assembly language for
speed." Chris Hodges, director of software at DSP-board vendor Atlantic
Signal Processing Inc(Atlanta, GA), agrees...have a real-time advantage
because next-generation RISC CPUs rely on complex memory hierarchies and
superscalar instruction scheduling. These techniques have performance
penalties for **cache misses** and interrupts that **limit**
determinism. Unlike RISC designers, DSP-chip developers live within the
constraints of restricted memory hierarchies, fast MAC cycles, and multiple
operations. But there's room...

16/3,K/13 (Item 13 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01550312   **Supplier Number:** 13279970 (Use Format 7 Or 9 For FULL TEXT)
**The first wave of Alpha AXP. (DEC's new computers based on Alpha microprocessor) (Special Report)(includes
related articles on application-specific-integrated-circuits in AXP systems) (Cover Story)**
Naecker, Philip A.
DEC Professional , v11 , n13 , p20(11)
Dec , 1992
Document Type: Cover Story
ISSN: 0744-9216
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 4846   **Line Count:** 00359
Abstract: ...improved speed and capacity, a 512Kbyte second-level cache and a new physical memory configuration. The
systems offer performance competitive with the fastest machines from **IBM**, Sun, HP and Silicon Graphics Inc. The
$69,900 DEC 4000 AXP minicomputer is designed as a departmental server but offers performance approaching that of...

...mirrors," he said.
    Within months, the VAX did ship, and it revolutionized the market for
computers of all sizes, eventually opening the glass house of **IBM**
systems by making powerful machines accessible and usable by ordinary
people. The VAX even defined a new class of computer -- the
superminicomputer. And the rigorous...board, while the Model 400 uses one
of the TURBOchannel slots for that purpose.
    Digital provides a 512-KB secondlevel cache on both systems to

reduce the impact of a **cache miss** on the relatively
small 8-KB cache onboard the 21064. Both systems are designed to be
uniprocessor systems only, which greatly simplifies the design of...
...also more expensive: $38,995. The Model 500 is priced to compete with
higher end graphics workstations, such as the fastest machines from Silicon
Graphics, **IBM**, Sun and HP.
On the other hand, few if any vendors can offer a machine that
matches the raw performance of the Model 500, so...

16/3,K/14 (Item 14 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01521158   Supplier Number: 12359791 (Use Format 7 Or 9 For FULL TEXT)
Intel's OverDrive raises the stakes for PC upgrades. (Hardware Review) (PC Week Special Report: X86 Choices -
A Brand-New Game) (Evaluation)
Chernicoff, David P.
PC Week , v9 , n25 , p116(2)
June 22 , 1992
Document Type: Evaluation
ISSN: 0740-1604
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 749   **Line Count:** 00057
Abstract: ...systems including an Acer America Corp AcerPower 486SX/25, an NCR Corp System 3335 486SX/25, a
GRiD Systems Corp MFP 420/S and an **IBM** PS/2 Model 90 425SX. Users should see a performance improvement of at
least 20 percent in 486SX systems upgraded with OverDrive. The most significant...

...selected from the 15 used to evaluate the OverDrive processors: an Acer
America Corp. AcerPower 486SX/25, a GRiD Systems Corp. MFP 420/S, an
IBM PS/2 Model 90 425SX and an NCR Corp. System 3335 486SX/25.
Lotus 1-2-3 showed the greatest performance improvement -- an average
increase...
...1 cache built into all Intel 486s acts as a buffer between the fast CPU
and slower dynamic RAM. This buffer can store only a **limited** amount
of information, and as **cache misses** occur the cache "hit
rate" falls precipitously.
While the clock-doubled 25MHz chips showed comparable performance to
the full-blown 50MHz 486DX in CPU and...

16/3,K/15 (Item 15 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01518696   Supplier Number: 12211560 (Use Format 7 Or 9 For FULL TEXT)
Buying power; a new motherboard can transform your old PC into a powerful new system. (includes related
articles on how to read a motherboard advertisement, what motherboards cost, and installation and radio
frequency interference problems)(includes representative list of motherboard vendors) (Tutorial)
Rowell, Dave
PC Sources , v3 , n6 , p238(10)
June , 1992
Document Type: Tutorial
ISSN: 1052-6579
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 5510   **Line Count:** 00407

...386 and 486 CPUs, you have a choice between motherboards that use the
16-bit industry standard architecture (ISA) expansion bus, a throwback to
the **IBM** PC AT, or the newer enhanced industry standard architecture
expansion bus, which can provide greater throughput and 32-bit data
transfers with special expansion cards...two in mind, start with board
size. There are two more-or-less standard board sizes, one based on the
size of motherboard in the **IBM** PC/XT, and one on the larger
motherboard found in **IBM's** XT AT. Boards following the XT form
factor are more often called baby AT boards, and are usually 8.5 by 13.5
inches...it pays to have memory that uses a page-mode or interleaved design
as a backup to caching. Many designs use both these tricks to **reduce**
wait states during **cache misses**.
You might also run across terms like direct-mapped, set associative,
and write-back to describe cache designs. Other than knowing that these
terms describe...

16/3,K/16 (Item 16 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01515075   Supplier Number: 12139084 (Use Format 7 Or 9 For FULL TEXT)
Optimizing your network for database rigors. (Network Solutions) (Tutorial)
O'Harra, Steven L.
Data Based Advisor , v10 , n5 , p93(9)
May , 1992
Document Type: Tutorial
ISSN: 0740-5200
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 4694   **Line Count:** 00368
Text:

...demands that both network administrators and database specialists
examine the cause/effect relationship of databases running on networks.
This article centers around NetWare and the **IBM**-compatible server.
For those in non-NetWare or heterogeneous environments, read on. These
issues and solutions are applicable to other platforms.

...of the write requests are handled in the background via the dirty cache
buffers (without the user seeing the delay). Large writes (beyond dirty
buffer **limits**) and **cache** "**misses**," on the other hand,
can work the drives to an early death and severely impact network
performance. A quick look at drives and their interface...

16/3,K/17 (Item 17 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01577124   Supplier Number: 14624575
How does processor MHz relate to end-user performance? Part 2: memory subsystem and instruction set.
(includes a related article on performance metrics) (Technical)
White, Steven W.; Hester, Phil D.; Kemp, Jack W.; McWilliams, G. Jeanette
IEEE Micro , v13 , n5 , p79(11)
Oct , 1993
Document Type: Technical
ISSN: 0272-1732
Language: ENGLISH   **Record Type:** ABSTRACT
Abstract: The first of the two-part series examined end-user performance by comparing the 62.5-MHz **IBM** RS/6000
Model 580 and the 160-MHz DEC Alpha; here the effect of memory subsystems and the instruction sets on path length
are studied to determine their performance implications. Cache designers make four primary choices when trying to
minimize the number of **cache misses**: set associativity, line size, capacity, and store policy. Simplifying cache design
makes high clock rates possible; among the options are smaller caches, direct-mapped caches...
Trade Names: IBM RS/6000 POWERServer 580 (Minicomputer...

16/3,K/18 (Item 18 from file: 148) <u>Links</u>
Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rights reserved.
06508167   Supplier Number: 14384363 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Forum opens Windows. (European Microprocessor Forum; Windows NT)
Manners, David
Electronics Weekly , n1640 , p12(1)
May 26 , 1993
Document Type: evaluation
ISSN: 0013-5224
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 931   **Line Count:** 00067

...this year but will say by first quarter 1994."
    Motorola's Mike Inglis laid out the masterplan for the new PowerPC
micros being developed by **IBM**, Apple and Motorola. The first of
these, the 601, is for the low-cost desktop market and is now being sold
for $280 a shot...
...66MHz versions could use 12ns SRAM. HP had decided not to integrate
cache on-chip because "on-chip caches have to be small and a **cache**
miss can be a primary performance **limiter**".
    By doing without on-chip cache the PA chip utilises only 800,000
transistors, reducing CPU die size -- "the most expensive silicon real

estate in...

16/3,K/19 (Item 19 from file: 88) <u>Links</u>
Gale Group Business A.R.T.S.
(c) 2007 The Gale Group. All rights reserved.
03378139   **Supplier Number: 16512390**
Commercial workload performance in the **IBM POWER2 RISC** System/6000 processor. (Performance Optimized With Enhanced RISC)
Franklin, M. T.; Alexander, W.P.; Jauhari, R.; Maynard, A.M.G.; Olszewski, B.R.
IBM Journal of Research and Development , v38 , n5 , p555(7)
Sept , 1994
ISSN: 0018-8646
Language: English   **Record Type:** Abstract
Commercial workload performance in the **IBM POWER2 RISC** System/6000 processor. (Performance Optimized With Enhanced RISC)
Abstract: The **IBM** Performance Optimized With Enhanced RISC 2 (POWER2) RISC System/6000 microprocessor optimizes system performance in an I/O-intensive commercial processing environment through an additional fixed-point instruction unit, cache size increase and cache line length increase. Reduced cycles per instruction increase transaction throughout. Cache modifications **minimize cache miss** rates.

16/3,K/20 (Item 20 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01674887   **Supplier Number: 15048613 (Use Format 7 Or 9 For FULL TEXT)**
ISSCC; digital technology. (International Solid State Circuits Conference)
Bursky, Dave
Electronic Design , v42 , n4 , p69(9)
Feb 21 , 1994
ISSN: 0013-4872
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 6194   **Line Count:** 00481

...delay variations comes from wiring delays, which forced NEC's designers
to come up with a new wiring architecture.
    VIRTUAL PORTS EASE DESIGN
    Designers at **IBM Corp.**, Essex Junction, Vt., describe a
virtual three-port memory array that can access three times in a 66-MHz bus
cycle. The array, which implements...function. When their functions aren't
needed, these state machines become idle by default and consume little
dynamic power.
    Continuing in this session, designers at **IBM** describe what
they did to spruce up the licensed 80386 architecture. Their efforts
produced a 66-MHz, 32-bit, 386-instruction-compatible procesosr that
delivers...
...enabled by special machine-specific registers.
    Many of the same power-saving techniques were applied to the PowerPC
family, as detailed by designers from the **IBM** Somerset Design
Center, Austin, Texas. Specifically, they talk about the 75 SPE-Cint/85
SPECfp supercalar RISC processor, the PowerPC603, released late last year.
Fabricated...
...of the company's latest 140-MHz 64-bit processor. The processor includes
a 64-entry (2-kbyte) full associative prefetch/miss cache that helps
reduce the effective **cache-miss** latency. Dual ALUs in
the chip's integer data path allow the processor execution, while
single-cycle load/store operations are possible to large off...

16/3,K/21 (Item 21 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01647938   **Supplier Number: 15936157**
Improving performance of linear algebra algorithms for dense matrices, using algorithmic prefetch.
Agarwal, R.C.; Gustavson, F.G.; Zubair, M.
IBM Journal of Research and Development , v38 , n3 , p265(11)
May , 1994
ISSN: 0018-8646
Language: ENGLISH   **Record Type:** ABSTRACT
Abstract: In this paper, we introduce a concept called algorithmic prefetching, for exploiting some of the features of the **IBM** RISC System/6000 computer. Alogirthmic prefetching denotes changing algorithm A to algorithm B, which contains additional steps to move data from slower levels of memory to faster levels, with the aim that algorithm B outperform algorithm A. The objective of algorithmic prefetching is to **minimize** any penalty due to **cache misses** in the innermost

loop of an algorithm. This concept, along with "cache blocking," can be exploited to improve the performance of linear algebra algorithms for...

16/3,K/22 (Item 22 from file: 148) <u>Links</u>
Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rights reserved.
07592601   **Supplier Number: 16497890 (USE FORMAT 7 OR 9 FOR FULL TEXT)**
Match 32- and 64-bit CPUs to embedded applications. (central processing unit) (Design Applications)
Terry, Dennis
Electronic Design , v42 , n24 , p105(7)
Nov 21 , 1994
ISSN: 0013-4872
Language: ENGLISH
Record Type: FULLTEXT; ABSTRACT
Word Count: 3861   **Line Count:** 00317
...Included are RISC families such as Sparc, MIPS, HP PA-RISC, Intel 960,
AMD 29000, DEC Alpha, and even the new PowerPC from Motorola and **IBM**
. Meanwhile, the proliferation of 32- and 64-bit CISC processors contenders
has slowed to a crawl--only Intel with its x86 family and Motorola with...
16-kbyte, four-way-set-associative caches. However, the
eight-way-set-associative design requires much more silicon real estate.
     Another useful cache feature that **minimizes** latency caused by
cache misses is the ability to lock specific time-critical
ISRs into the cache. For example, the new 68060 processor includes dual
8-kbyte data and instruction...

16/3,K/23 (Item 23 from file: 47) <u>Links</u>
Gale Group Magazine DB(TM)
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04204747   **Supplier Number: 16553701 (USE FORMAT 7 OR 9 FOR FULL TEXT)**
Micron's Millennia proves to be fastest PC. (100MHz Pentium system) (Hardware Review) (Evaluation)
Knorr, Eric
PC World , v13 , n3 , p56(1)
March , 1995
Document Type: Evaluation
ISSN: 0737-8939
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 354   **Line Count:** 00028
Abstract: ...Pentium processor, as the fastest PC to date. The system comes with 16MB of Extended Data Out (EDO)
memory, which uses a new technique to **reduce** performance lags caused by **cache misses**. Cache misses occur when
a processor cannot find data it needs in the primary or secondary cache and cause wait states. EDO avoids wait states...
...in a PC to keep up--including system memory. That's why Micron, a major
system vendor and the only domestic memory chip manufacturer besides
IBM, decided to build innovative memory technology into its new P100
Millennia system. The result? Nothing less than the fastest PC you can buy
today.
     When...

16/3,K/24 (Item 24 from file: 16) <u>Links</u>
Gale Group PROMT(R)
(c) 2007 The Gale Group. All rights reserved.
03888574   **Supplier Number: 45595818 (USE FORMAT 7 FOR FULLTEXT)**
Larger caches planned for 604
Electronics Times , p 6
June 8 , 1995
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 186
(USE FORMAT 7 FOR FULLTEXT)
Text:

IBM and Motorola are planning to launch an enhanced version of
their PowerPC 604 processor with larger caches and a higher clock rate
using a 0...
 The move follows similar improvements in the 603e and 601e processors, but
the 604 is the processor for Apple's PowerMac computers and **IBM's**
PCs running NT and 0S/2 Warp, and also for embedded applications. Intel is
currently making its high-end Pentium processors on 0.35m.
     The caches will be increased from two 16kbyte caches, in the existing
design, to two of 32kbyte, which will **reduce** the **cache**

miss rate and so improve performance.
    The clock will be increased from 100 to 150MHz, giving a total
performance of around 220Spec92Int. The power consumption at...
...is expected to be around the same as the existing 100MHz 604 at 8 to 9W.
    The existing design of 604 is being moved from **IBM**'s CMOS5L
five-layer 0.5m process to CMOS5S, with a smaller effective gate length to
increase the yields. But the enhanced 604 will be...
Company Names:
***International Business Machines** Corp.; Motorola Inc.

16/3,K/25 (Item 25 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01822641   Supplier Number: 17172619 (Use Format 7 Or 9 For FULL TEXT)
Inside the P6. (aggressive design of new Intel P6 microprocessor) (includes related article on how P6 bus is optimized for speed and multiprocessing)
Stam, Nick
PC Magazine , v14 , n15 , p118(8)
Sep 12 , 1995
ISSN: 0888-8507
Language: English   **Record Type:** Fulltext; Abstract
Word Count: 5499   **Line Count:** 00439

...fastest L2-cache subsystems in most Pentium systems typically impose at
least two wait states when a memory access misses in the L1 cache.
    To **minimize** the performance penalty associated with
cache misses further, the L1 and L2 caches of the P6 are both
nonblocking. When information that the processor needs is not contained in
either cache, that...
...In fact, the bus controller on the P6 contains 89,000 transistors--far
more circuitry than on the entire 8088 processor that powered the original
IBM PC.)
    Support for a delayed-response mechanism gives system designers the
ability to extend the P6 beyond four-way multiprocessing. In particular, it
enables a...

16/3,K/26 (Item 26 from file: 16) <u>Links</u>
Gale Group PROMT(R)
(c) 2007 The Gale Group. All rights reserved.
05295113   Supplier Number: 48062477 (USE FORMAT 7 FOR FULLTEXT)
Deep-submicron design challenge unfolds at Microprocessor Forum: Keep execution units busy -- Complex RISC collides with IA-64 parallelism
Wolfe, Alexander; Wilson, Ron
Electronic Engineering Times , p 1
Oct 20 , 1997
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 1622

...they want on a high-power die, the problem is keeping all those
functional blocks busy.
    On the RISC front, new processors from Hewlett-Packard, **IBM**
Microelectronics and Sun Microelectronics offered potential solutions in
the form of multiple integer-execution pipes, multiple floating-point
pipes, and separate load/store and branch...
...latency can be a more- expensive problem. Architects' first line of
defense has been to build big, single-cycle L1 caches, in an attempt to
minimize the number of L1 **cache misses**. But the
hardware cost of this approach is growing. HP's PA-8500, for example, has
1.5 Mbytes of L1 cache on-chip. The company has described the 8500 as a
cache SRAM with an ancillary CPU. Taking a different approach, the
IBM Power3 design team included only 32 kbytes of instruction and 64
kbytes of data cache, but made each cache 128-way set associative.
    Another way to reduce the miss rate is to cheat. Instruction sets in
both Sun's Sparc V9 and **IBM**'s Power3 include prefetch instructions
that, in effect, tell the CPU to preload certain information into its L1
caches.
    Trying to overcome branches can lead...

16/3,K/27 (Item 27 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
02046695   Supplier Number: 19226876 (Use Format 7 Or 9 For FULL TEXT)
MMX muscle machines. (12 Pentium MMX-based PCs reviewed) (includes related articles on other products reviewed that did not arrive in time, how products were tested, how MMX technology works) (Hardware Review)(Evaluation)
Broida, Rick
Computer Shopper , v16 , n4 , p130(11)
April , 1997
Document Type: Evaluation
ISSN: 0886-0556
Language: English   **Record Type:** Fulltext; Abstract
Word Count: 7106   **Line Count:** 00569
...applications, MMX-enabled or not. The most significant improvements
include doubling the L1 cache size to 32K (16K for data and 16K for
instructions) to **reduce cache misses**, and improving
the chip's instruction pairing so it can process two instructions per cycle
more frequently.
     Tested with our non-MMX-enabled Business Winstone...system's, the
Comtrade's case features a slide-out chassis for easy access to the
motherboard. All ports are conveniently labeled.
     The 2.1GB **IBM** Deskstar 3's performance was topped only by the
Sys Performance system's. Likewise, the 12x Toshiba XM-5702B CD-ROM batted
an out-of...fastest in the group, the Dell scored higher than most other
similarly equipped systems at 800x600 in true-color mode. The Dell's 3.2GB
IBM Deskstar 3 hard drive was one of the faster performers of the
group and offers a good amount of disk space. Not surprisingly, the Dell...
roundup. The MidWest Micro's 12x Mitsumi CD-ROM drive turned in
above-average scores, however, and we liked the spaciousness of the 3.2GB
IBM hard drive, which delivered a slightly below-average Disk
WinMark 97 score.
     Superbly equipped for multimedia, the Home PC features a three-piece
Altec Lansing...

16/3,K/28 (Item 28 from file: 9) <u>Links</u>
Business & Industry(R)
(c) 2007 The Gale Group. All rights reserved.
01390878 Supplier Number: 24059784 **(USE FORMAT 7 OR 9 FOR FULLTEXT)**
Deep-submicron design challenge unfolds at Microprocessor Forum: Keep execution units busy -- Complex RISC collides with IA-64 parallelism
(Complex twists on traditional RISC-based superscalar CPUs competed with Intel's new, highly parallel IA-64 architecture at Microprocessor Forum)
Electronic Engineering Times , p 01
October 20, 1997
Document Type: Journal **ISSN:** 0192-1541 (United States)
Language: English **Record Type:** Fulltext
Word Count: 1586 **(USE FORMAT 7 OR 9 FOR FULLTEXT)**
ABSTRACT:
...they want on a high-power die, the problem is keeping all those functional blocks busy. On the RISC front, new
processors from Hewlett-Packard, **IBM** Microelectronics and Sun Microelectronics offered potential solutions in the form of
multiple integer-execution pipes, multiple floating-point pipes, and separate load/store and branch...
TEXT:

On the RISC front, new processors from Hewlett-Packard, **IBM**
Microelectronics and Sun Microelectronics offered potential solutions in
the form of multiple integer-execution pipes, multiple floating-point
pipes, and separate load/store and branch...
...latency can be a more- expensive problem. Architects' first line of
defense has been to build big, single-cycle L1 caches, in an attempt to
minimize the number of L1 **cache misses**. But the
hardware cost of this approach is growing. HP's PA-8500, for example, has
1.5 Mbytes of L1 cache on-chip. The company has described the 8500 as a
cache SRAM with an ancillary CPU. Taking a different approach, the
IBM Power3 design team included only 32 kbytes of instruction and
64 kbytes of data cache, but made each cache 128-way set associative.
Another way to reduce the miss rate is to cheat. Instruction sets in both
Sun's Sparc V9 and **IBM**'s Power3 include prefetch instructions that,
in effect, tell the CPU to preload certain information into its L1 caches.

Trying to overcome branches can lead...

16/3,K/29 (Item 29 from file: 647) **Links**
CMP Computer Fulltext
(c) 2007 CMP Media, LLC. All rights reserved.
01141878   **CMP Accession Number: EET19971020S0017**
Deep-submicron design challenge unfolds at Microprocessor Forum: Keep execution units busy - Complex RISC collides with IA-64 parallelism
Ron Wilson and Alexander Wolfe
ELECTRONIC ENGINEERING TIMES , 1997 , n 976 , PG01
Publication Date: 971020
Journal Code: EET **Language:** English
Record Type: Fulltext
Section Heading: News
Word Count: 1633

...they want on a high- power die, the problem is keeping all those
functional blocks busy.
     On the RISC front, new processors from Hewlett-Packard, **IBM**
Microelectronics and Sun Microelectronics offered potential solutions in
the form of multiple integer-execution pipes, multiple floating- point
pipes, and separate load/store and branch...
...latency can be a more- expensive problem. Architects' first line of
defense has been to build big, single-cycle L1 caches, in an attempt to
minimize the number of L1 **cache misses**. But the
hardware   cost of this approach is growing. HP's PA-8500, for example, has
1.5 Mbytes of L1 cache on-chip. The company has described the 8500 as a
cache SRAM with an ancillary CPU. Taking a different approach, the
IBM Power3 design team included only 32 kbytes of instruction and
64 kbytes of data cache, but made each cache 128-way set associative.
     Another way to reduce the miss rate is to cheat. Instruction sets in
both Sun's Sparc V9 and **IBM**'s Power3 include prefetch
instructions that, in effect, tell the CPU to preload certain information
into its L1 caches.
     Trying to overcome branches can lead...

16/3,K/30 (Item 30 from file: 148) **Links**
Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rights reserved.
09820874   **Supplier Number:** 19927446 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Complex RISC collides with IA-64 parallelism. (Intel's IA-64 64-bit processor architecture is described at the Microprocessor Forum) (Company Business and Marketing)
Wilson, Ron; Wolfe, Alexander
Electronic Engineering Times , n976 , p1(2)
Oct 20 , 1997
ISSN: 0192-1541
Language: English
Record Type: Fulltext; Abstract
Word Count: 1776   **Line Count:** 00142
Abstract: Intel's highly parallel IA-64 64-bit microprocessor architecture shared center stage with new RISC-based superscalar CPUs from HP, **IBM** Microelectronics and Sun Microelectronics at the Microprocessor Forum in San Jose, CA, in Oct 1997. HP and Intel worked together on the unique IA-64 ...

...they want on a high-power die, the problem is keeping all those
functional blocks busy.
     On the RISC front, new processors from Hewlett-Packard, **IBM**
Microelectronics and Sun Microelectronics offered potential solutions in
the form of multiple integer-execution pipes, multiple floating-point
pipes, and separate load/store and branch...
...latency can be a more- expensive problem. Architects' first line of
defense has been to build big, single-cycle L1 caches, in an attempt to
minimize the number of L1 **cache misses.** But the
hardware cost of this approach is growing. HP's PA-8500, for example, has
1.5 Mbytes of L1 cache on-chip. The company has described the 8500 as a
cache SRAM with an ancillary CPU. Taking a different approach, the
IBM Power3 design team included only 32 kbytes of instruction and 64
kbytes of data cache, but made each cache 128-way set associative.
     Another way to reduce the miss rate is to cheat. Instruction sets in

both Sun's Sparc V9 and IBM's Power3 include prefetch instructions
that, in effect, tell the CPU to preload certain information into its L1
caches.
    Trying to overcome branches can lead...

16/3,K/31 (Item 31 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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02180984   Supplier Number: 20738163 (Use Format 7 Or 9 For FULL TEXT)
Greater expectations.(CMOS technology to make next generation of IBM mainframes more powerful) (Company
Business and Marketing)
Enticknap, Nick
Computer Weekly , p30(1)
May 7 , 1998
ISSN: 0010-4787
Language: English   Record Type: Fulltext
Word Count: 869   Line Count: 00070
Greater expectations.(CMOS technology to make next generation of IBM mainframes more powerful) (Company
Business and Marketing)
Text:

It looks like good news for **IBM** mainframe users for a change, as
performance gains from the latest CMos technology are set to deliver beyond
expectations.

IBM's next generation of mainframes could be significantly more
powerful than the company has so far suggested. Karl Strassemeyer, product
planning manager at **IBM**'s Boblingen Laboratory, hinted to Computer
Weekly that Generation 5 of **IBM**'s 9672 CMos mainframe line will have
a uniprocessor of at least 100 mips (millions of instructions per second),
and possibly more, rather than the 90 mips that **IBM** executives have
previously promised.
    Strassemeyer said that "the G5 uniprocessor is practically equal to
Skyline". Skyline is the hybrid bipolar-CMos mainframe developed by Hitachi
...
...powerful than we have so far been hearing. The party line is that G5
will have one-and-a-half times the power of H5, **IBM**'s last bipolar
mainframe. That gives about 90 mips, so these two performance claims flatly
contradict each other.
    Which is the more likely to be...
...following different mainframe technology development paths since 1992,
and each needs to convince its customers it has gone for the right option.
    In that year **IBM** abandoned the bipolar logic circuitry that had
been used in all powerful mainframes for over 20 years, to concentrate
instead on the rival CMos technology...
...dissipation, and is developing at a much faster rate than bipolar
systems
    Less power
    The snag is that, in 1992, it delivered much less power. **IBM**'s
first mainstream CMos mainframe, the 9672-Ri launched in 1994, had a
uniprocessor of just 14 mips, compared with the contemporary **IBM**
bipolar uniprocessor of 61 mips. So to provide its bipolar mainframe users
with a growth path, **IBM** introduced a clustering technology known as
parallel sysplex.
    Hitachi decided to follow a different path, and developed a hybrid
bipolar-CMos technology called Ace (Advanced...
...Skyline has proved successful, allowing the Hitachi companies to claim
20% of the mainframe market in 1996, and a similar or greater proportion in
1997. **IBM** has been forced to acknowledge the success of the system
by acquiring one of its own for its System Recovery Centre in Maryland: the
press release announcing this on **IBM**'s Web site acknowledges the
"efficient system management" capabilities of Skyline.
    So **IBM** needs to show that its own CMos developments are rapidly
closing the gap on Skyline, and Strassemeyer's claim must be seen in this
context.
    A major jump forward is all the more important because **IBM**'s
1997 CMos mainframe, Generation 4, was rather a disappointment.
    Performance down
    This was to have been the generation that would equal or exceed the...
...but multiprocessor performance was substantially less.

Strassemeyer admits this, but claims the performance shortfall "is nothing to do with processor design". Instead, "our anticipation of **cache misses** was 10% **lower**: with the memory bus being loaded, these little differences create quite a big deviation."

That was not the only problem. The top-end model, the RY5, would not deliver the necessary power without overheating, so a cooler had to be developed. This attracted criticism from analysts at the time, but **IBM** has since turned it to its advantage.

"We are maturing this technology right now," says Strassemeyer, "so as to run chips faster, even if we...

...to achieve extra power.

Reading between the lines, it is hard not to conclude that G4 was a production engineering disaster. For instance, in March **IBM** abandoned its original plan for the 1999 generation, which was to have been a superscalar version of G4. Instead, this generation will be created by...
Company Names:
International Business Machines Corp...

16/3,K/32 (Item 32 from file: 88) <u>Links</u>
Gale Group Business A.R.T.S.
(c) 2007 The Gale Group. All rights reserved.
05391266　**Supplier Number:** 60269931
Static Correlated Branch Prediction.
YOUNG, CLIFF; SMITH, MICHAEL D.
ACM Transactions on Programming Languages & Systems , 21 , 5 , 1028
Sept , 1999
ISSN: 0164-0925
Language: English　　**Record Type:** Fulltext
Word Count: 20377　**Line Count:** 01713

...semantics. Transforming a control-flow graph into a linear sequence of instructions is called the code layout problem; algorithms that attack code layout attempt to **reduce cache misses** or pipeline stalls in the program by changing the order of basic blocks or procedures (Calder and Grunwald 1994; Hwu and Chang 1989; McFarling 1993...University. Cliff Young was supported in part by a National Defense Science and Engineering Graduate Fellowship from the Office of Naval Research and by an **IBM** Cooperative Fellowship. Michael D. Smith is funded in part by a NSF Young Investigator award (grant no. CCR-9457779), NSF grant no. CDA-94-01024, DARPA grant no. NDA904-97-C-0225; and research grants from AMD, Compaq, Digital Equipment, HP, **IBM**, and Intel. Authors' addresses: C. Young, Lucent Technologies, 700 Mountain Avenue, Room 2C-523, Murray Hill, NJ 07974; email: cyoung@research.bell-labs.com; M...

16/3,K/33 (Item 33 from file: 88) <u>Links</u>
Gale Group Business A.R.T.S.
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05391265　**Supplier Number:** 60269930
Procedure Placement Using Temporal-Ordering Information.
GLOY, NIKOLAS; SMITH, MICHAEL D.
ACM Transactions on Programming Languages & Systems , 21 , 5 , 977
Sept , 1999
ISSN: 0164-0925
Language: English　　**Record Type:** Fulltext
Word Count: 20310　**Line Count:** 01723

...postcompilation tools, and that it is orthogonal to other techniques to arrange code within procedures.

Our procedure-placement technique improves the instruction cache mapping to **reduce** the number of instruction **cache misses** in one or multiple levels of instruction cache. In addition, our approach considers the effect of the code placement on other levels of the memory...suffer from repeated misses on that cache line, even if there are other available cache lines that are not used at that moment. Such a **cache miss** that is caused by the **restrictive** cache mapping is known as a conflict miss.

2.1.3 Identifying a Metric Related to Conflict Misses. By moving pieces of the code within...show how to extend our TPCM algorithm to

simultaneously optimize code placement in multiple levels of the cache
hierarchy. Our results show that we can **reduce cache
misses** in all cache levels while retaining virtually all of the
first-level cache performance.

5.1 Impact of L1 Placement on the L2 Cache

Since...AND DONALDSON, D. 1996. AlphaServer 4100 performance
characterization. Digital Technical Journal 8, 4, 3-20.

CYTRON, R. AND LOEWNER, P. 1986. An automatic overlay generator.
IBM Journal of Research and Development 30, 6 (Nov.), 603.

DENNING, P. 1970. Virtual memory. Computing Surveys 2, 3 (Sept.),
153-189.

FERRARI, D. 1974. Improving locality by critical working sets.
Commun. ACM 17, 11 (Nov.), 614-620.

FERRARI, D. 1975. Tailoring programs to models of program behavior.
IBM Journal of Research and Development 19, 244.

GLOY, N., BLACKWELL, T., SMITH, M. D., AND CALDER, B. 1997. Procedure
placement using temporal ordering information. In...
...SIGPLAN '97 Conference on Programming Language Design and
Implementation. ACM, New York, 171-182.

HATFIELD, D. AND GERALD, J. 1971. Program restructuring for virtual
memory. **IBM** Systems Journal 10, 3, 168-192.

HILL, M. D. 1988. A case for direct-mapped caches. Computer 21, 12
(Dec.), 25-40.

HWU, W. AND...Proceedings of the 21st Annual International Symposium
on Computer Architecture. IEEE, Los Alamitos, California, 372-383.

RYDER, K. 1974. Optimizing program placement in virtual systems.
IBM Systems Journal 13, 292.

SMITH, A. 1982. Cache memories. Computing Surveys 14, 3 (Sept.),
473-530.

SMITH, J. AND HSU, W.-C. 1992. Prefetching in...
...no. CCR-9457779), NSF grant no. CDA-94-01024, DARPA grant no.
NDA904-97-C-0225, and research grants from AMD, Compaq, Digital Equipment,
HP, **IBM**, and Intel.

The research reported in this article was conducted while the first
author was a graduate student in the Division of Engineering and Applied...

16/3,K/34 (Item 34 from file: 88) <u>Links</u>
Gale Group Business A.R.T.S.
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05389173   **Supplier Number: 60589366**
Quantifying Loop Nest Locality Using SPEC'95 and the Perfect Benchmarks.
McKINLEY, KATHRYN S.; TEMAM, OLIVIER
ACM Transactions on Computer Systems , 17 , 4 , 288
Nov , 1999
ISSN: 0734-2071
Language: English   **Record Type:** Fulltext
Word Count: 15551   **Line Count:** 01402

...which is orthogonal to the above:
-- Compulsory Misses: Misses that occur on the first reference to a
block.
-- Capacity Misses: Additional misses resulting from the
limited capacity of a **cache.**
-- Conflict **Misses:** Additional misses due to mapping
constraints in set-associative caches.

Like Hill, we measure conflict and capacity misses with respect to a
fully associative cache...J. L. Martin, Ed. ACM Press, New York, NY,
176-186.

BELADY, L.A. 1966. A study of replacement algorithms for a
virtual-storage computer. **IBM** Syst. J. 5, 2, 79-101.

BODIN, F., BECKMAN, P., GANNON, D., GOTWALS, J., NARAYANA, S.,
SRINIVAS, S., AND WINNICKA, B. 1994. Sage++: An object...

16/3,K/35 (Item 35 from file: 88) <u>Links</u>
Gale Group Business A.R.T.S.
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05315471   **Supplier Number: 59473656**
Cache Miss Equations: A Compiler Framework for Analyzing and Tuning Memory Behavior.(computer memory)(Statistical
Data Included)

GHOSH, SOMNATH; MARTONOSI, MARGARET; MALIK, SHARAD
ACM Transactions on Programming Languages & Systems , 21 , 4 , 703
July , 1999
Document Type: Statistical Data Included
ISSN: 0164-0925
Language: English   **Record Type:** Fulltext
Word Count: 21263   **Line Count:** 01741

...representing all the cache misses in a loop nest. This simple, precise
characterization allows one to better understand the cause behind such
misses, and helps **reduce cache misses** in a methodical
way.
     CMEs are unique in unifying both the loop structure and the data
layout within a simple, equations-based analytical model representing...
mathematical properties of the CMEs. We illustrate this with the help of
two examples. The first example shows how the CMEs can be used to
reduce cache misses by changing the base addresses and
the column sizes (i.e., padding) of the arrays referenced. The second
example shows how the equations can be...to the upper bound of the loop
index hu.
     Equations (14) and (15) have 232 and 269 solutions respectively. Each
solution corresponds to a potential **cache miss.** We wish to
reduce the number of solutions in order to reduce the cache
interferences represented by these equations. We intend to do that by
changing the base addresses...help us to analyze and optimize loops with
parametric loop bounds.
     7.3 Applications
     As described in Section 5, the CMEs can be used to **reduce** the
number of **cache misses** due to their precise characterization
of the cache misses. Also, the CMEs provide users with a general framework
from which different kinds of optimizations to...491-542.
     BACON, D. F. ET AL. 1994. A compiler framework for restructuring data
declarations to enhance cache and TLB effectiveness. In Proceedings of the
IBM Centre for Advanced Studies Conference '94.
     BAILEY, D. 1992. Unfavorable strides in cache memory systems. Tech.
Rep. RNR-92-015, NASA Ames Research Center, CA...eliminate cache conflicts.
In Proceedings of the Supercomputing'93 Conference.
     TORRELLAS, J., LAM, M. S., AND HENNESSEY, J. L. 1990. Shared data
placement optimizations to **reduce** multiprocessor **cache**
miss rates. In Proceedings of the 1990 International Conference on
Parallel Processing.
     WILSON, R. P. ET AL. 1994. SUIF: An infrastructure for research on
parallelizing and...

 16/3,K/36 (Item 36 from file: 16) <u>Links</u>
Gale Group PROMT(R)
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07962215   **Supplier Number: 66170635 (USE FORMAT 7 FOR FULLTEXT)**
EEMBC 1.0 SCORES, PART 2 : Analysis & Mysteries.(Industry Trend or Event)
Levy, Markus
Microprocessor Report , v 14 , n 9 , p 28
Sept , 2000
Language: English   **Record Type:** Fulltext
Document Type: Newsletter ; Trade
Word Count: 3157
...and its associated data fit into the caches. For those benchmarks that
do not fit into the caches, performance profiling will reveal the number of
cache misses and the corresponding benefits or
limitations of the memory subsystem.
     VRSO00 Floating Point Blows Doors Off Others
     For most of the EEMBC automotive/industrial benchmarks, we observed
that AMD's 450MHz...
...the K6-2 is 35% and 59% slower, respectively. Another indicator of the
VRS000's strong floatingpoint capability appeared when we compared this
processor with **IBM's** 500MHz PowerPC 750CX, which executes three
times faster on the benchmarks in this suite, except for the floating-point
and matrix-arithmetic benchmarks, where...
...the 64-bit results. In addition, the K6 executes floating-point
instructions in a minimum of two processor clocks, whereas the maximum is

significantly higher. **IBM**'s 750CX contains a 64-bit FPU that can pipeline up to three instructions. Most of its floating-point instructions execute with three- or fourcycle...benchmarks.

Processor Name	Clock rate (MHz)	Native Compiler	Data Type
AMD ElanSC520	133	CAD-UL I381G1X0	32
AMD K6-2	450	CAD-UL I381G1X0	32
IBM PowerPC 750CX	500	Wind River Diab 4.3b	32
IDT79RC32364	100 and 150	Algorithmics SDE4.0B	32
IDT79RC64575	250	Algorithmics SDE4.0B	64

Infineon TriCore...

Processor Name	FPU	I/D Cache	I/D Cache Type
AMD ElanSC520	Yes	16K/16K	2-way SA
AMD K6-2	Yes	32K/32K	2-way SA
IBM PowerPC 750CX	Yes	32K/32K	8-way SA
IDT79RC32364	No	8K/2K	2-way SA
IDT79RC64575	Yes	32K/32K	2-way SA
Infineon TriCore	No...		

...2-way SA

Processor Name	L2 Cache Clock	Bus Width	Bus Freq. (MHz)
AMD ElanSC520	n/a	32	66
AMD K6-2	66	32	66
IBM PowerPC 750CX	500	64	66
IDT79RC32364	n/a	32	50
IDT79RC64575	n/a	64	50
Infineon TriCore TC10GP	n/a	32	80
Mitsubishi	n/a...		

16/3,K/37 (Item 37 from file: 88) <u>Links</u>

...1994).
    The poor locality of accesses to the server reduces the effectiveness of increasing the server cache size. Adding more memory to the server does **reduce** the **cache miss** rate, but adding enough memory to achieve a significant effect is prohibitively expensive. Furthermore, as the server cache tends to duplicate the contents of the...cache always

replaces the block whose next access is farthest in the future. It has been
shown that this replacement policy is optimal because it **minimizes**
the number of **cache misses** and therefore has the minimal
block access time (Belady 1966).
　　The Optimal replacement algorithm must be slightly modified for use
in a cooperative cache. There...AND MAGNUS, R. 1996. Linux Kernel
Internals. Addison-Wesley, Reading, MA.
　　BELADY, L. A. 1966. A study of replacement algorithms for a
virtual-storage computer. **IBM** Syst. J. 5, 2, 79-101.
　　CACERES, R., DUFFIELD, N., FELDMANN, A., GREENBERG, J. D., GREER, A.,
JOHNSON, R., KALMANEK, T., KRISHNAMURTHY, C. R., LAVELLE...Conference
(June). 127-138.
　　Received: June 1998; revised: January 2000 and July 2000; accepted:
September 2000

' Authors' addresses: P. Sarkar, Storage Servers and Systems
Department, **IBM** Almaden Research Center, 650 Harry Road, San Jose,
CA 95120; J. H. Hartman, Department of Computer Science, The University of
Arizona, Tucson, AZ 85721.

...Section 4 reports on an evaluation of an industry-leading HPF compiler
from the Portland Group Inc. using the HPFBench benchmarks on the
distributed-memory **IBM** SP2. Finally, Section 5 summarizes the
article.
　　2. THE HPFBENCH METHODOLOGY
　　2.1 Language Aspects
　　The HPFBench benchmark codes are written entirely in High Performance
...suite is provided to enable testing the performance of
compiler-generated code against that of a highly optimized library, such as
the ESSL and PESSL (**IBM** 1996) for the **IBM** SP2. Performance
attributes for the linear algebra codes are presented in Tables V-VII,
tabulating the data representation and layout for dominating kernel
computations, the...
...codes represent the best performance tuning effort from low-level
programming. Message passing implementations of LU, QR factorizations, and
matrix-vector multiplication are available from **IBM**'s PESSL library
(**IBM** 1996), and in other libraries such as ScaLAPACK (Blackford et
al. 1997) from University of Tennessee, among others. However, the
functions in such libraries often...the time-dominant computation kernels
of large applications, and often hand-optimized as mathematical library
functions by the supercomputer vendors (e.g., ESSL and PESSL (**IBM**
1996) from **IBM**). These hand-optimized implementations attempt to
make efficient use of the underlying system architecture through efficient
implementation of interprocessor data motion and management of local...
lu--and six from application kernels -- ellip-2d, fem-3d, mdcell,
pic-simple, pic-gather-scatter, and rp.
　　4. EVALUATION RESULTS OF PGHPF ON THE **IBM** SP2
　　We report on the results of evaluating an industry-leading HPF
compiler, pghpf, from the Portland Groups, Inc., on the distributed-memory
IBM SP2, using all 25 benchmarks in the HPFBench suite. Version
2.2-2 of pghpf with compiler switch -O3 -W0, -O4 was used and linked...
...and the performance of the sequential code compiled using the native
Fortran 77 compiler, xlf, with compiler flag -O4.
　　Our evaluation was performed on an **IBM** SP2 with 16
uniprocessor nodes. Each node has a RS6000 POWER2 Super Chip processor
running AIX 4.3 at 120MHz and has 128MB of main memory. The nodes are
communicating through **IBM**'s MPL library on the **IBM** SP2
high-performance switch network with a peak node-to-node bandwidth of

150MB/ second. All results were collected under dedicated use of the
machines...
...problem sizes of the benchmarks as listed in Table XIII for the
evaluation, due to the relative small main memory on each node of the
IBM SP2.

4.1 Linear Algebra Functions

4.1.1 Sequential Performance. Table XV compares the the performance
of the linear algebra benchmark codes compiled using...
...benchmarks shows that the improvement is due to the default padding
(-Moverlap=size:4) by pghpf along all parallel dimensions of an array which
reduces **cache** conflict **misses** by from a **moderate**
amount in fft-3d and lu:nopivot to a significant amount in pcr:inst...have
reported a performance evaluation of an industry-leading HPF compiler,
pghpf, from the Portland Group Inc. using the HPFBench benchmarks on the
distributed-memory **IBM** SP2. While with respect to running the HPF
benchmarks on one node, most of the benchmarks achieved good speedups on up
to 16 nodes of...Symposium on Principles and Practice of Parallel
Programming (SIGPLAN '97, Las Vegas, NV, June 18-21), M. A. Berman, Ed. ACM
Press, New York, NY.

IBM. 1996. IBM Parallel Engineering and Scientific
Subroutine Library Release 2, Guide and Reference. **IBM Corp.,**
Riverton, NJ.

JOHNSON, C. 1987. Numerical Solutions of Partial Differential
Equations by Finite Element Method. Cambridge University Press, New York,
NY.

JOHNSON, C. AND SZEPESSY...

16/3,K/39 (Item 39 from file: 996) <u>Links</u>
NewsRoom 2000-2001
(c) 2006 Dialog. All rights reserved.
0173034206 158U11EX
A multithreaded PowerPC processor for commercial servers
Borkenhagen, J M
IBM Journal of Research & Development , v 44 , n 6 , p 885
Thursday , November 30, 2000
Journal Code: AERK **Language:** ENGLISH **Record Type:** Fulltext
Document Type: Scholarly Journal **ISSN:** 0018-8646
Word Count: 9,928
Text:

This paper describes the microarchitecture of the RS64 IV, a multithreaded
PowerPC processor, and its memory system. Because this processor is used
only in **IBM** iSeries(TM) and pSeries(TM) commercial servers, it is
optimized solely for commercial server workloads. Increasing miss rates
because of trends in commercial server applications...

...The operating frequency of SStar was increased to 600 MHz compared with
Northstar's 262-MHz debut. This increase in frequency was accomplished by
leveraging **IBM**'s CMOS 8S copper and silicon-on-insulator (SOI)
technology, along with redesign of timing-critical paths. The LI I-cache
and L1 D-cache...
...cache directory was integrated into the processor chip.
The processor die, containing 44 million transistors, is shown in Figure 1.
It is manufactured in the **IBM** 1.5-V 0.18-mu m copper CMOS 8S
technology, with seven levels of copper interconnect. The processor has the
following attributes:
- Two-way...added to the 6XX bus transaction tag ID. The thread bit is
returned on the bus with cache-miss data.
Various techniques were used to **minimize** the L1 D-**cache**
miss penalty to eight cycles. The L2 SRAM clocking logic is designed
to tolerate a wide range in access delays caused by SRAM process variation
without...
...is implemented with SRAMs external to the processor chip. The external
L2 cache is four-way set associative. Associativity in the L2 results in
significantly **lower** L2 **cache-miss** rates for commercial
server workloads. In a four-way associative cache, all four directory
entries and all four data blocks are usually accessed in parallel...with
other performance-improvement techniques, multithreading yields an
excellent ratio of performance gain to implementation cost.

Memory thougput improve from multithreading

References
1. http://www.specbench.org.
2. A. Maynard, C. Donnelly, and B. Olzewski, "Contrasting Characteristics
...Eds., Morgan Kaufmann Publishers, San Francisco, 1994.
15. http://www.tpc.org.

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Minnesota 55901 (bork@us.ibm.com). Dr. Borkenhagen is a Senior
Technical Staff Member with **IBM** Server Development in Rochester,
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coherency, hardware multithreading, and storage control architecture.
Richard J. Eickemeyer **IBM** Server Group, 3605 Highway 52 N,
Rochester, Minnesota 55901 (eick@us.ibm.com). Dr. Eickemeyer is a
Senior Engineer in the **IBM** Server Group. He is currently the
processor core performance team lead for **IBM**'s PowerPC servers.
Prior to this, he worked on performance and architecture for several
processors used in AS/400 systems and S/390 systems in Rochester,
Minnesota, and Endicott, New York. Since joining **IBM**, he has
received awards which include the Seventh Plateau **IBM** Invention
Achievement Award, an Outstanding Technical Achievement Award, an
Outstanding Innovation Award, and a Corporate Award for Hardware
Multi-Threading. He has also been named...
...S. and Ph.D. degrees from the University of Illinois at
Urbana-Champaign. His research interests are computer architecture and
performance analysis.
Ronald N. Kalla **IBM** Server Group, 11400 Burnet Road, Austin, Texas
78758 (rkalla@us.ibm.com). Mr. Kalla is a Senior Engineer with
IBM Server Development, Austin, Texas. In 1983 he joined **IBM**
in Endicott, New York, where he worked on mid-range System/370 processors.
In 1989, he transferred to Rochester, Minnesota, to work on AS/400...
...on the POWER4 processor, which will be used in future pSeries servers.
Mr. Kalla's interests are in processor architecture and performance.
Steven R. Kunkel **IBM** Server Group, 3605 Highway 52 N, Rochester,
Minnesota 55901 (srkunkel@us.ibm.com). Dr. Kunkel received his Ph.D.
degree from the University of Wisconsin at Madison in 1987. He then joined
IBM in Endicott, New York, doing performance analysis of a vector
facility for a mid-range S/390 product. In 1989, he transferred to
Rochester, Minnesota...
...Kunkel is currently a Senior Technical Staff Member doing architecture
and performance analysis for iSeries (AS/400), pSeries (RS/6000), and
xSeries (Netfinity) servers.

16/3,K/40 (Item 40 from file: 996) <u>Links</u>
NewsRoom 2000-2001
0127034444   155Y11NC
EEMBC 1.0 SCORES, PART 2 : Analysis & Mysteries.
Snyder, Cary D.
Microprocessor Report , v 14 , n 9 , p 20
Friday , September 1, 2000
Journal Code: AAQU **Language:** ENGLISH **Record Type:** Fulltext
Document Type: Newsletter **ISSN:** 0899-9341
Word Count: 3,257

...and its associated data fit into the caches. For those benchmarks that

do not fit into the caches, performance profiling will reveal the number of
cache misses and the corresponding benefits or
limitations of the memory subsystem.
VRSO00 Floating Point Blows Doors Off Others
For most of the EEMBC automotive/industrial benchmarks, we observed that
AMD's 450MHz...
...the K6-2 is 35% and 59% slower, respectively. Another indicator of the
VRS000's strong floatingpoint capability appeared when we compared this
processor with IBM's 500MHz PowerPC 750CX, which executes three
times faster on the benchmarks in this suite, except for the floating-point
and matrix-arithmetic benchmarks, where...
...the 64-bit results. In addition, the K6 executes floating-point
instructions in a minimum of two processor clocks, whereas the maximum is
significantly higher. IBM's 750CX contains a 64-bit FPU that can
pipeline up to three instructions. Most of its floating-point instructions
execute with three- or fourcycle...benchmarks.

Processor Name	Clock rate (MHz)	Native Compiler	Data Type
AMD ElanSC520	133	CAD-UL I381G1X0	32
AMD K6-2	450	CAD-UL I381G1X0	32
IBM PowerPC 750CX	500	Wind River Diab 4.3b	32
IDT79RC32364	100 and 150	Algorithmics SDE4.0B	32
IDT79RC64575	250	Algorithmics SDE4.0B	64
Infineon TriCore...			

	...FPU	I/D Cache	I/D Cache Type	
AMD ElanSC520	Yes	16K/16K		2-way SA
AMD K6-2	Yes	32K/32K	2-way SA	
IBM PowerPC 750CX	Yes	32K/32K		8-way SA
IDT79RC32364	No	8K/2K	2-way SA	
IDT79RC64575	Yes	32K/32K		2-way SA
Infineon TriCore	No...2-way SA			

Processor Name	L2 Cache Clock	Bus Width	Bus Freq. (MHz)
AMD ElanSC520	n/a	32	66
AMD K6-2	66	32	66
IBM PowerPC 750CX	500	64	66
IDT79RC32364	n/a	32	50
IDT79RC64575	n/a	64	50
Infineon TriCore TC10GP	n/a	32	80
Mitsubishi	n/a...		

16/3,K/41 (Item 41 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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02618135   **Supplier Number: 87508144 (Use Format 7 Or 9 For FULL TEXT)**
Let caches decay: reducing leakage energy via exploitation of cache generational behavior.
Hu, Zhigang; Kaxiras, Stefanos; Martonosi, Margaret
ACM Transactions on Computer Systems , 20 , 2 , 161(30)
May , 2002
ISSN: 0734-2071
Language: English   **Record Type:** Fulltext; Abstract
Word Count: 12361   **Line Count:** 00964

...access and the point where a new data item is brought into that cache
location. Turning off the cache line during this dead period can
reduce leakage, without introducing any additional **cache**
misses and without hurting performance.
   We propose several policies for determining when to turn off a cache
line. We begin with a time-based strategy, which...
...2 to 5% of power dissipation (or even higher (Butts and Sohi 2000)), but
it is expected to grow exponentially in upcoming generations (Borkar 1999;
IBM Corp. 2000; Semiconductor Industry Association 1999).
   2.2 Leakage Power and Cache Generations
   Because caches comprise much of the area in current and future
microprocessors, it...into the future. In such cases, it may be
power-optimal to shut off the cache line early, mark it as invalid, and
accept a **moderate** increase in the number of **cache**
misses. Later sections offer more realistic policies for managing

these trade-offs. On the other hand, real-world attempts to put cache lines
to sleep will...are orthogonal and synergistic with other "helper" caches
such as victim caches or stream buffers. These other caching structures can
be helpful as ways of **mitigating** the **cache miss**
increases from cache decay, without as much leakage power as larger
structures.

6.4 DRAM Caches

Some recent work has discussed the possibility of DRAM...E. G. AND
REINHARDT, S. K. 2000. A fully associative software-managed cache design.
In Proceedings of the 27th International Symposium on Computer Architecture
(June).

IBM CORP. 2000. Personal communication. November.

INTEL CORP. 1997. Intel architecture optimization manual.

KAMBLE, M. B. AND GHOSE, K. 1997. Analytical energy dissipation
models for low power...
...In Proceedings of the 22nd International Symposium on Computer
Architecture.

SAIR, S. AND CHARNEY, M. 2000. Memory behavior of the SPEC2000
benchmark suite. Tech. Rep., **IBM**.

SEMICONDUCTOR INDUSTRY ASSOCIATION. 1999. The International
Technology Roadmap for Semiconductors. Available at
http://www.semichips.org.

STALLINGS, W. 2001. Operating Systems. Prentice-Hall, Englewood
Cliffs...

16/3,K/42 (Item 42 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
02618133   Supplier Number: 87508142 **(Use Format 7 Or 9 For** FULL TEXT)
The evolution of Coda.
Satyanarayanan, M.
ACM Transactions on Computer Systems , 20 , 2 , 85(40)
May , 2002
ISSN: 0734-2071
Language: English   **Record Type:** Fulltext; Abstract
Word Count: 18730   **Line Count:** 01514

...hence, users are given more control. As bandwidth rises, delays shrink
and the annoyance from interaction dominates; hence, more cases are handled
transparently. In the **limit**, at strong connectivity, **cache**
misses are fully transparent.

On a cache miss, Venus first invokes the model with the file name,
current bandwidth, and other system information as parameters. If...were
eager to freely distribute Coda, we discovered that it was legally viewed
as "derived code" and could not be distributed without the permission of
IBM, the owner of AFS-2. The long and frustrating process of
obtaining this permission was made more difficult by the fact that we could
offer no tangible benefit in return. To **IBM**'s credit, our request
was eventually honored. Between 1992 and 1995, the code was distributable
for research and educational purposes but an explicit license had to be
signed by each recipient. After a further round of negotiation in late
1995, **IBM** finally released control of Coda. Only then were we able
to freely distribute Coda through the Internet.

The long delay in making Coda freely available...in this article into
a single system.

A secondary reason for Coda's longevity has been the near-absence of
commercial systems with similar capabilities. **IBM** Transarc, the
custodian of AFS, would have been the most likely candidate to build a
commercially supported distributed file system along the lines explored by
...
...improve it. Bill Tetzlaff, Dejan Milojicic, and the anonymous journal
reviewers also offered valuable suggestions to improve the presentation.

Major support was also provided by **IBM**, Digital Equipment, and
Intel. Additional support was provided by AT&T, Bellcore, General
Electric, Hughes Research, Novell, Sun Microsystems, and Xerox. The views
and conclusions...CSD-900010, University of California, Los Angeles, April.

HARRISON, E. S. AND SCHMITT, E. J. 1987. The structure of System/88,
a fault-tolerant computer. **IBM** Syst. J. 26, 3.

HENNESSY, J. 1999. The future of systems research. IEEE Computer 32,
8 (August).

HERLIHY, M. P. 1986. A quorum-consensus replication...

16/3,K/43 (Item 43 from file: 995) <u>Links</u>
NewsRoom 2002
(c) 2006 Dialog. All rights reserved.
0536581016   15ZK2H3R
Tying up a MIPS32 processor with threads: Lexra evolves LX4380 pipeline into multithreading processor.(Hardware Review)(Product/Service Evaluation)
Levy, Markus
Microprocessor Report , v 16 , n 11 , p 34(4)
Friday , November 1, 2002
Journal Code: AAQU **Language:** English **Record Type:** Fulltext
Document Type: Newsletter **ISSN:** 0899-9341
Word Count: 2,692
Text:

...its Hyper-Threading technology in Pentium 4, providing groundbreaking
innovation for the PC industry (although similar technology has been around
since the early days of **IBM** mainframes). Other processors, such as
Intel's IXP and **IBM**'s NP4GS3 (see MPR 01/02/01-01, "Rainier Leads
PowerNP Family") are also examples of multithreading-capable processors.
Lexra's LX4580 is the most...

...better than a conventional singled-threaded processor. Nevertheless,
Lexra claims the HMT has a performance advantage when the cache miss rate
exceeds 2% or when **cache miss** latency exceeds 50ns. T o
reduce complexity, the processor's bus interface will support one
instruction-cache miss and one data-cache miss for each thread.
Tying Off the Threads
Not...
...other embedded-processor vendors (IP or silicon) show up in 2003 with
some form of HMT. In fact, we recommend that vendors such as ARM,
IBM, MIPS, and SuperH, start offering multithreaded cores to
increase the efficiency of their architectures.
In addition to the challenges associated with adopting HMT, Lexra also...
...have led various VLSI development projects in the past. But in the
markets it is targeting, Lexra is going up against many powerful
hitters--Broadcom, **IBM**, Intel, Motorola, PMC Sierra, and others
having years of manufacturing experience. That noted, it must be said that
many companies do switch from IP to...

16/3,K/44 (Item 44 from file: 995) <u>Links</u>
NewsRoom 2002
(c) 2006 Dialog. All rights reserved.
0454531289   15UF0YKS
Response to Shahin Khan's "Wolf in Sheep's Clothing":
Client Server News (UK) , n 452
Monday , May 27, 2002
Journal Code: AHBJ **Language:** English **Record Type:** Fulltext
Document Type: Trade Journal **ISSN:** 1351-5500
Word Count: 3,556
...this has never been more apparent.
I responded to your original letter - not because of blind love for Linux
and/or naive misunderstandings of the **IBM** zSeries strategy - but
because my work involves research on open standards, "mainframes" based on
Intel processors and dynamic partitioning technology with fair sharing of
all...
...open standards." However, that was decades ago and there are new
challenges to face:
Sun can't win in the niche Unix market against HP, **IBM** and SGI
because Sparc/Solaris servers are perceived as "general-purpose" Unix
servers and now, with the rise of Linux, are not perceived as "open...
...Windows dominates "Closed Systems." Each category can only support one
major player.
Although Sun now has a Linux offering, you are likely to lose to **IBM**
, whose success is driven by **IBM** Global Services, the world's most
expansive technical services organization. Without a strong service
organization, Sun finds itself unable to profitably embrace high-end Linux

...

...this is an attempt to confuse the business community and the truth is
that Linux businesses are real and thus a real threat to Sun. **IBM**
invests in Linux to make money. Red Hat, SuSE, Caldera, Turbolinux and
SWsoft also invest in Linux to make money. Linux is not an altruistic...

...fair sharing of system resources, including memory and CPU. Sun's
Dynamic System Domains lack the fair-sharing features found in LPAR and VM
on **IBM**'s mainframes. These fair-sharing dynamic partitioning
features are common on Linux on Intel with technologies such as
carrier-grade Virtuozzo for Linux. Data centers...

...size is also not true. The mainframe's shared cache can be considerably
smaller than the dedicated cache on Sun's servers because of the
lower cache missed rate of shared cache systems. The
size of the mainframe's processor cache is perfectly sized for the
mainframe's processors, as additional cache would...

...mainframes needed more processor cache, the cache size of the mainframe
could easily be increased. Additional processor cache could be added quite
cheaply. The reason **IBM** doesn't add more processor cache is because
it's not needed.

You also didn't mention that shared cache enables hardware to survive CPU

20/3,K/1 (Item 1 from file: 15) <u>Links</u>
ABI/Inform(R)
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00575025   91-49374
IBM's 386SX Releases Heat Up Low-End Market
Uiterwijk, Andreas; Van Cura, Jeff; Kaliczak, Anne
InfoWorld   v13n40 pp: 72
Oct 7, 1991
ISSN: 0199-6649 Journal Code: IFW
Word Count: 816
Text:

...low-end office workstations and potential OS/2 platforms.
IBM Model 35SX
PRODUCT SUMMARY
Company: IBM Corp., 1133 Westchester Ave., White Plains, NY 10604; (800)
IBM-9292.
List Price: $3,020 (standard configuration plus an additional 2 megabytes
of RAM); sold through dealer channels.
Features: 20-MHz zero-wait-state 80386SX...
...one serial, one parallel, one mouse port; VGA adapter built in; Intel
80387SX or compatible math coprocessor support; 197-watt power supply.
Peripherals: Enhanced keyboard; **IBM** 16-bit VGA built-in.
Storage and Memory: 40-megabyte Maxtor hard disk with 1:1 controller (our
tests were run with an 80-megabyte drive); 1.44-megabyte 3-1/2-inch floppy
drive; 4 megabytes of 80-nanosecond **RAM** (16 megabytes **maximum**
.)
IBM PS/2 Model 40SX
PRODUCT **SUMMARY**
Company: **IBM Corp.**, 1133 Westchester Ave., White Plains, NY
10604; (800) **IBM**-9292.
List Prke: $3,690 as configured; sold through dealer channels.
Features: 20-MHz zero-wait-state 80386SX CPU; one serial, one parallel, one
mouse port; VGA adapter built in; Intel 80387SX or compatible math
coprocessor support; 197-watt power supply.
Peripherals: Enhanced keyboard; **IBM** 16-bit VGA built-in.
Storage and Memory: 80-megabyte Maxtor hard disk with built-in ESDI 1:1
controller; 1.44-megabyte 3-1...

20/3,K/2 (Item 2 from file: 15) <u>Links</u>
ABI/Inform(R)
(c) 2007 ProQuest Info&Learning. All rights reserved.
00552675   91-27032
IBM Hits the Ground Running with Clever 486SX-Based PC
Zittle, Tim; Kaliczak, Anne
InfoWorld   v13n21 pp: 93-94
May 27, 1991
ISSN: 0199-6649 Journal Code: IFW
Word Count: 892
Text:
...24 evaluation; the scores reported in this review could change at that
time due to the relative performance of other 486SX computers.
PRODUCT SUMMARY
Company: **IBM Corp.**, Old Orchard Road, Armonk, NY 10604; (800)
IBM-2468.
List Price: $8,945 as configured; sold through dealer channels, authorized
industry remarketers, and marketing representatives.
Features: 20-MHz 80486SX CPU; XGA adapter; built...
...serial, one parallel, one PS/2 mouse port; Intel 80487SX math
coprocessor support; 194-watt power supply.
Peripherals: Enhanced keyboard.
Storage and Memory: 160-megabyte **IBM** hard disk with SCSI 1:1
controller and 256K of disk cache; 1.44-megabyte 3-1/2-inch floppy drive; 4
megabytes of 70-nanosecond RAM (SIMMs on expandable daughterboards, 32
megabytes **maximum**); 8K of **RAM** cache on the 486SX chip.
Pros: Small footprint, low **profile**; simple disassembly; large SCSI
storage options; built-in XGA.
Cons: Slim manual; patches on CPU daughter board.
Summary: The Model 90 XP 486SX is a...

20/3,K/3 (Item 3 from file: 15) <u>Links</u>
ABI/Inform(R)
(c) 2007 ProQuest Info&Learning. All rights reserved.
00544442   91-18787
Product Comparison: 25-MHz 386 Workhorse PCs
Garza, Victor R.; Price, Jerome; Zittle, Tim; Kvitka, Andre; Smith, Gregory S.; Petreley, Nicholas; Capen, Tracey
InfoWorld   v13n13 pp: 45-58
Apr 1, 1991
ISSN: 0199-6649 Journal Code: IFW
Word Count: 3441
Text:

...we've seen in other Vectra models, but it is solidly constructed and
relatively fast. Its price is comparatively high among units in this
comparison.
IBM PS/2 Model 70 386/25 A-21
PRODUCT SUMMARY
Company: **IBM Corp.**, 1133 Westchester Ave., White Plains, NY
10604; (800) IBM-2468. List Price: $7,340 as configured; sold
through dealer channels. Features: 25-MHz zero-wait-state 80386 CPU; VGA
adapter, serial, parallel, and mouse ports built-in; Intel or compatible
math coprocessor support; 132-watt power supply. Peripherals: Enhanced
keyboard. Storage and Memory: 120-megabyte **IBM** hard disk with
built-in ESDI 1:1 controller; 1.44-megabyte 3-1/2-inch floppy drive; 4
megabytes of 80-nanosecond **RAM** (SIMMS, 16 megabytes **maximum**);
64K of 20-nanosecond **RAM** cache. Pros: Small footprint, low
profile; simple disassembly. Cons: Slowest CPU and disk speed; .
limited expandability; thin documentation; dealer-only support. Summary:
IBM's Model 70, the only Micro Channel system in this comparison,
has two things going for it – its small size and the **IBM** label.
It's also the most expensive system of the group.
NEC PowerMate 386/25S   ·
PRODUCT SUMMARY
Company: NEC Technologies Inc., 1414 Massachusetts Ave., Boxborough...

20/3,K/4 (Item 1 from file: 647) <u>Links</u>
CMP Computer Fulltext
(c) 2007 CMP Media, LLC. All rights reserved.
01053974   **CMP Accession Number:** OEM19950501S0005
WRONG BIOS, WRONG RAM
OEM MAGAZINE , 1995 , n 317 , PG10
Publication Date: 950501
Journal Code: OEM **Language:** English
Record Type: Fulltext
Section Heading: Letters
Word Count: 118
Text:

...February issue and wish to make one small correction to the ``Inside
Information" department (page 74). The Panasonic CF-41 notebook computer
listed in the **chart** uses the **IBM** BIOS version 2.0L10, and
the **maximum RAM** is now 48 Mbits (16 Mbits base plus a
32-Mbit card). Also, the unit has been shipping since early March (in
Canada) in a...

20/3,K/5 (Item 1 from file: 20) <u>Links</u>
Dialog Global Reporter
(c) 2007 Dialog. All rights reserved.
23023650 **(USE FORMAT 7 OR 9 FOR FULLTEXT)**
Enterprise Week - Servers add mainframe tools.
Server hardware report Roger Howorth.
IT WEEK , p 25
May 27, 2002
Journal Code: WVNU **Language:** English   **Record Type:** FULLTEXT
Word Count: 539
(USE FORMAT 7 OR 9 FOR FULLTEXT)

...RAM disk fitted in the NetVista. ·
    Most sites will link the NetVista to the server using a standard
serial interface, but the NetVista also runs **IBM**'s WebSM system

management tool, so the server can be managed remotely via the NetVista
using a suitable browser or telnet link.
  Server partitioning tools make use of IBM's mainframe heritage
of logical partitions. A basic logical partition comprises a boot disk
and an Ethernet adapter. IBM's workload Manager tool supports
multiple profiles for each of the logical partitions. A profile defines
the other resources associated with each partition, such as the minimum
and **maximum** processors and **RAM**, and which PCI I/O slots are
used. Switching between **profiles** is not yet fully automated, though
it is expected to be in version 5.2 of AIX, which is due this year.
  - www.**ibm**.com/eservers
  SUMMARY
  - **IBM**'s new pSeries servers are among the first mid-range
systems with mainframe features.
  - The p670 and p690 use the same 24in chassis as **IBM**
mainframes.
  - They also have similar partitioning tools, and features to cut
downtime.

 20/3,K/6 (Item 2 from file: 20) **Links**
Dialog Global Reporter
(c) 2007 Dialog. All rights reserved.
03514354 **(USE FORMAT 7 OR 9 FOR FULLTEXT)**
IBM: IBM announces SAP certification of its DataInterchange interface
M2 PRESSWIRE
November 20, 1998
Journal Code: WMPR **Language:** English **Record Type:** FULLTEXT
Word Count: 561
(USE FORMAT 7 OR 9 FOR FULLTEXT)

...to reduce the number of trading partner profiles. Trading partner
profile and usage setup is simplified, eliminating the need to define an
individual trading partner **profile** for each partner.
  Other enhancements include pageable translation for **memory
optimization**, full standards compliance checking and increased
DataInterchange Client functionality. For more information on
DataInterchange visit, http://delilah.fl.us.**ibm**
.net/datainterchange/.
  With 1997 revenues of approximately $26 billion, **IBM** Global
Services is the world's largest information technology services provider.
IBM's fastest growing business segment has an unsurpassed breadth of
capabilities, and more than 118,000 professionals helping companies of all
sizes solve real business problems and create new business opportunities.
For more information on **IBM** Global Services, visit http://www.
ibm.com/services.
  *M2 COMMUNICATIONS DISCLAIMS ALL LIABILITY FOR INFORMATION PROVIDED
WITHIN M2 PRESSWIRE. DATA SUPPLIED BY NAMED PARTY/PARTIES.*

 20/3,K/7 (Item 1 from file: 275) **Links**
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
02538143   **Supplier Number: 78268665 (Use Format 7 Or 9 For** FULL TEXT)
TOP 10 PRINTERS.(Buyers Guide)
PC World , 19 , 10 , 181
Oct , 2001
Document Type: Buyers Guide
ISSN: 0737-8939
Language: English   **Record Type:** Fulltext
Word Count: 350   **Line Count:** 00138

...E312   Very good/
    find.pcworld.com/11670   .   Adequate
    CORPORATE LASER
    1 (Best BUY)   Very good/
    Xerox DocuPrint N2125   Very good
    find.pcworld.com/11600
    2 IBM Infoprint 21   Very good/
    find.pcworld.com/11660   Good
    3 HP Laser Jet 4100n   Excellent/

find.pcworld.com/11661   Good

20/3,K/8 (Item 2 from file: 275) Links
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
02476360   Supplier Number: 70652492 (Use Format 7 Or 9 For FULL TEXT)
TOP 10 PRINTERS.(Hardware Review)(Evaluation)
PC World , 19 , 3 , 185
March , 2001
Document Type: Evaluation
ISSN: 0737-8939
Language: English   Record Type: Fulltext; Abstract
Word Count: 422   Line Count: 00144

20/3,K/9 (Item 3 from file: 275) Links
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
02373820   Supplier Number: 59555415 (Use Format 7 Or 9 For FULL TEXT)
TOP 100 Old Concept, New Look: All-in-One PCs.(Hardware Review)(Evaluation)

20/3,K/10 (Item 4 from file: 275) Links
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01367566   Supplier Number: 08821844 (Use Format 7 Or 9 For FULL TEXT)
IBM ES/390.
Computergram International , n1507 , CGI09070012
Sept 7 , 1990
ISSN: 0268-716X
Language: ENGLISH   Record Type: FULLTEXT
Word Count: 1042   Line Count: 00078

...4391", the Model 480 has over 4.0 times internal performance of the
4381-92E in commercial work.
     i b m
     One of the problems IBM has created with its new numbering
schema is that in referring to the new models, one has to keep unravelling
it to understand what one...
...based on the pre-announcement information is an invaluable guide, and we
reprint it below - with the memory and channels added and the errors
corrected!
     Summary of ES/9000 announcement
     Model Processors MIPS(e) Maximum Max Escon, memory std
chnnls Summit 9021-900 Six 212 9Gb 256 9021-820 Four 161 9Gb 256
     3090 9021-720 Six 112 4.5Gb 128 9021-620...

20/3,K/11 (Item 5 from file: 275) Links
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01291124   Supplier Number: 07348173 (Use Format 7 Or 9 For FULL TEXT)
Buyer's Guide features chart. (80386-based IBM-compatible 20- to 33MHZ microcomputers) (buyers guide)
Lee, Charlene
Personal Computing , v13 , n3 , p185(6)
March , 1989
Document Type: buyers guide
ISSN: 0192-5490
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 267   Line Count: 00021
Abstract: A chart, listing features of 80386-based IBM-compatible microcomputers operating at CPU clock speeds
ranging from 20- to 33MHz, is provided. The chart's columns include: CPU clock speed, base memory and maximum
RAM, BIOS manufacturer, RAM cache, power supply in watts, number of expansion slots, number of drives supported,
and any bundled software available with the system.

20/3,K/12 (Item 1 from file: 47) Links
Gale Group Magazine DB(TM)
(c) 2007 The Gale group. All rights reserved.
05211697   Supplier Number: 21049062 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Top 20 Power Desktop PCs.(Micron Electronics' Millennia 400 and 350, and Gateway's GP6/400 top the list of
power Pentium II-based systems) (Hardware Review)(Evaluation)
PC World , v16 , n9 , p194(1)

Sep , 1998
Document Type: Evaluation
ISSN: 0737-8939
Language: English   **Record Type:** Fulltext
Word Count: 8013   **Line Count:** 00599
...the 400BA to rack up such a high benchmark score. All the basic hardware
is top-notch, including the 8.4MB Deskstar hard drive from **IBM** and
the Sound Blaster AWE64 sound card. The Matrox Millennium II AGP video card
may not be on our Top 10 list, but it's...
...more expansion room. (You still get two open DIMM sockets with this
configuration, but even three sockets wouldn't let you upgrade to the
listed **maximum** of 1GB of **RAM**--the most on the power
chart--without replacing all the DIMMs.) The 400BA comes with no
bundled software beyond the operating system and the normal system drivers.
And the included user...

20/3,K/14 (Item 1 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01322269   **Supplier Number: 41539283 (USE FORMAT 7 FOR FULLTEXT)**
IBMES/3 9 0
Computergram International , n 1506 , p N/A
Sept 7 , 1990
Language: English   **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 955

...end dual processor "4391", the Model 480 has over 4.0 times internal
performance of the 4381-92E in commercial work.
    One of the problems **IBM** has created with its new numbering
schema is that in referring to the new models, one has to keep unravelling
it to understand what one...
...based on the pre-announcement information is an invaluable guide, and we
reprint it below - with the memory and channels added and the errors
corrected!
    Summary of ES/9000 announcement
    Model Processors MIPS(e) **Maximum** Max Escon, **memory** std
chnnls Summit 9021-900 Six 212 9Gb 256 9021-820 Four 161 9Gb 256
    3090 9021-720 Six 112 4.5Gb 128 9021-620...

20/3,K/15 (Item 1 from file: 148) <u>Links</u>
Gale Group Trade & Industry DB
(c)2007 The Gale Group. All rights reserved.
05023254   **Supplier Number: 10683960**
**IBM air-cooled mainframes raising the high water mark. (product evaluation)(includes related article Viewpoints:
Cowboys and engines) (editorial)**
Brady, Sharon
Infoperspectives , p1(9)
March , 1991
Document Type: editorial
ISSN: 0733-9305
Language: ENGLISH
Record Type: CITATION
Captions: IBM air-cooled mainframes salient characteristics. (table); Share of machines using the **maximum** amount of
main **memory**. (chart); The value of the 4381 base has declined. (graph); 9121S are already visible in the population.
(chart); 9121S provide nearly a third of the MIPS...

31/3,K/1 (Item 1 from file: 15) <u>Links</u>
ABI/Inform(R)
(c) 2007 ProQuest Info&Learning. All rights reserved.
01298661   99-48057
SOHO & more
Anonymous
Dealerscope Consumer Electronics Marketplace   v38n7 pp: 19-20
Jul 1996
ISSN: 0888-4501 Journal Code: DEA
Word Count: 845
Text:

...personal organizer line offers an INDIGLO night-light and data
synchronization feature. The one-touch feature updates and reconciles data
between the organizer and an **IBM**-compatible PC. The organizers range
from $110 to $195 SRP and begin shipping this month. The **Model**
PS6965Si bundle ($239 SRP) offers **maximum memory** (256KB), a
PC Connectivity Kit with docking station and Windows software for
synchronization. Circle 107.
ROYAL'S ORGANIZER
WITH RADIO
ROYAL'S Model BG98 organizer...

 31/3,K/2 (Item 2 from file: 15) <u>Links</u>
ABI/Inform(R)
(c) 2007 ProQuest Info&Learning. All rights reserved.
00355829   87-14663
Mainframes: IBM Moves to Take the High Ground
Moad, Jeff
Datamation   v33n6 (OEM Edition) pp: 22, 26
Mar 15, 1987
ISSN: 0011-6963 Journal Code: DAT
Abstract:

...memory components to the 5890 line, while National Advanced Systems
plans to accelerate initial shipment of the AS/XL 90 and AS/XL 100 and
boost maximum main **memory** on both **models.**
IBM hopes to challenge Amdahl's 41MIPS 5890-300 dual processor
system with its new 3090-300E. While some large users, like United
Airlines, say the...

 31/3,K/3 (Item 3 from file: 15) <u>Links</u>
ABI/Inform(R)
(c) 2007 ProQuest Info&Learning. All rights reserved.
00338235   86-38649
IBM 'Fixes' System/36 as Part of Product Blitz
Haber, Lynn
Mini-Micro Systems   v19n11 pp: 43-48
Sep 1986
ISSN: 0364-9342 Journal Code: MOD
Abstract:

...System/36 product line includes the high-end 5360 model D, and the
mid-size 5362 models B and C, both of which provide a **maximum** of 2M
bytes of **memory.** IBM also replaced System/38 **models**
4, 6, 18, 20, and 40 with 6 new computers. The low end of those
replacements is the model 100 with 2M bytes of memory...

 31/3,K/4 (Item 1 from file: 9) <u>Links</u>
Business & Industry(R)
(c) 2007 The Gale Group. All rights reserved.
01423935 Supplier Number: 24097734 **(USE FORMAT 7 OR 9 FOR FULLTEXT)**
The Mega-Notebook Makes a Big Splash
(International Business Machines Corp introduces ThinkPad 770 notebook; Micron introduces Transport XKE 233 notebook)
Windows Magazine , v 8 , n 12 , p 136+
December 1997
Document Type: Journal **ISSN:** 1060-1066 (United States)
Language: English **Record Type:** Fulltext
Word Count: 1168

ABSTRACT:
...TFT) screen, respectively. Both come with 32MB of RAM, and a Trident Cyber 9397 accelerated graphics controller with 2MB of video memory. This unit supports **IBM**'s UltraBay, which can accept an additional battery, a 3.5-in floppy disk drive, 20X **(maximum)** CD-**ROM** drive or DVD drive.The **Model** 9549-1AU comes wiht the Intel P55C 233MHz processor, a 5.1GB hard drive and a 14.1-in display. The Micron Transport XKE 233...

31/3,K/5 (Item 1 from file: 635) <u>Links</u>
Business Dateline(R)
(c) 2007 ProQuest Info&Learning. All rights reserved.
0479279   94-32980
AS/400 goes on the road; IBM announces new portable AS/400 for customers
McNair, Barbara
Business Wire (San Francisco , CA , US) s 1 p 1
Publication Date: 940321
Word Count: 757
Dateline: White Plains, NY, US
Text:

...and interoperability, and has been continually upgraded and expanded to
become the most popular business system in the world.
   (a) Trademark or registered trademark of **International**
Business Machines Corporation.
  March 21, 1994
      PORTABLE ONE **MODEL** P02 SPEC SHEET
     Base **memory**   8MB
     Maximum memory   16MB
     Base DASD   1GB
     Maximum DASD   2GB
     Communications Lines   1
     Maximum addresses   3
     Weight   21 lbs / 9.5Kg
                 (maximum configuration)
     Size (HxDxW)   13x16x4" / 32x40x10cm
     Preloaded software   OS/400 Version 2...

31/3,K/6 (Item 1 from file: 610) <u>Links</u>
Business Wire
(c) 2007 Business Wire. All rights reserved.
00363786   20000914258B9737 (USE FORMAT 7 FOR FULLTEXT)
IBM Breaks From the Pack with New NetVista Desktop PCs; New models deliver edge-of the-network capabilities; complete product transition to sleek-designed, easy-to-use systems
Business Wire
Thursday , September 14, 2000   14:44 EDT
Journal Code: BW **Language:** ENGLISH **Record Type:** FULLTEXT **Document Type:** NEWSWIRE
Word Count: 1,207

...b) (up to 633, 667 or 700 MHz (1), depending on the model) or
Intel Pentium III (800, 866 or 933 MHz, depending on the **model**)
processors,
with 128 MB of **SDRAM** standard (up to a **maximum** of 512 MB).
Additionally, the
The Build Your Own A40i models feature the latest AMD Athlon and Duron
processors.
IBM also announced today a new model of its NetVista X40i all-in-one
PC. Now
available with Microsoft's Windows Millenium Edition, the X40i features...

31/3,K/7 (Item 1 from file: 810) <u>Links</u>
Business Wire
(c) 1999 Business Wire . All rights reserved.
0014597   BW164
IBM 2 : Strengthens mid-range connectivity; introduces new System/36 and System/38 models, workstations, controllers and pc-to-mainframe link
June 16, 1986
Byline: Business Editors

...addition,
it offers 7 megabytes (MB) of main memory, 3-1/2 times more than
the current model.

The new System/36 mid-size 5362 **models** B and C provide a
maximum of 2MB main **memory**
-- double that available with current
models. The model C can operate with the **IBM**
9332 direct access
storage device, a new disk file announced today. One or two
files can be attached, providing an additional 200MB or 400MB of...

31/3,K/8 (Item 1 from file: 647) <u>Links</u>
CMP Computer Fulltext
(c) 2007 CMP Media, LLC. All rights reserved.
00510073 **CMP Accession Number: EET19920727S2942**
IBM goes Hollywood
ALEXANDER WOLFE
ELECTRONIC ENGINEERING TIMES , 1992 , n 703 , 16
Publication Date: 920727
Journal Code: EET Language: English
Record Type: Fulltext
Section Heading: News
Word Count: 406

...the introduction of the PVS Model 4 Server. The parallel-processing
system incorporates 32 Intel i860XP CPUs and as much as 2.5 Gbytes of
memory. In addition, the **maximum** system **memory** in PVS
models 1, 2 and 3 was increased from 1.5 to 2.5 Gbytes.
      IBM also extended the multiuser capability of PVS servers to
handle up to eight users simultaneously.
      In the software arena, IBM introduced an improved version of...

31/3,K/9 (Item 1 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
02300158   **Supplier Number: 54732247 (Use Format 7 Or 9 For** FULL TEXT)
HDS Gets Its Eight-Way NT Server Away.
Computergram International , NA
May 26 , 1999
ISSN: 0268-716X
Language: English   **Record Type:** Fulltext
Word Count: 298   **Line Count:** 00026
Text:

...server generally available. HDS did its own implementation of Intel
Corp's Corollary Profusion chipset which is driving other eight-ways, which
gave it early **samples** as well **boosting** Profusion's
memory throughput to 1.6Gbps from 1.3Gbps. VisionBase is available
with 500MHz Pentium III Xeons now - 550MHz CPUs next quarter. **IBM**,
Compaq, Dell HP and others expect to have eight-way NT servers using
Profusion boards out later this summer. Other vendors, including Unisys
Corp, have...

31/3,K/10 (Item 2 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01705978   **Supplier Number: 16306428 (Use Format 7 Or 9 For** FULL TEXT)
486/Now!: MCMaster. (Kingston Technology) (one of five evaluations of seven CPU upgrades from "Processor
Upgrades: New Life for Your Old PC?") (Hardware Review) (Evaluation)
Anthony, Robert S.
PC Magazine , v13 , n19 , p147(2)
Nov 8 , 1994
Document Type: Evaluation
ISSN: 0888-8507
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 785   **Line Count:** 00064

...can now remove the floppy disk and reboot your machine.
      On our Winstone test, the MCMaster MC50PD/8 upgrade board, aided by
its 8MB of **RAM**, helped **boost** the **IBM PS/2 Model**
55's score by 265 percent. But, like other CPU upgrades in this roundup,

the MCMaster board caused a slight dip in the IBM PS...

31/3,K/11 (Item 3 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01557098   Supplier Number: 12079116 (Use Format 7 Or 9 For FULL TEXT)
IBM raises the bar with 2 new machines. (Big Blue's 386 SX machines, the PS/2 25 SX and PS/2 57 SLC, aimed at the education market, a good value, but the cost of the high-end multimedia option, which will run Columbus and Ulysses - may cause educators evaluate carefully) (Hardware Review) (includes related article on IBM's Educational Systems division, now called Eduquest; another related article describes the hardware needed to run Columbus and the Illuminated Books and Manuscripts series) (Evaluation)
Brady, Holly
Technology & Learning , v12 , n6 , p34(4)
March , 1992
Document Type: Evaluation
ISSN: 1053-6728
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 1611   Line Count: 00133

...least expensive and the least powerful machine in the PS/2 line. Its
microprocessor is the low-end 8086 chip, and it comes with a **maximum**
of 640K of **memory**.
    The new **Model** 25 SX is scheduled to ship next month.
    A New High-End Multimedia Machine
    But when you think of **IBM**'s multimedia efforts, you
automatically think of the company's ambitious Columbus and Ulysses
projects. These beautiful and highly complex programs have been
demonstrated by...

31/3,K/12 (Item 4 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01492830   Supplier Number: 11678382 (Use Format 7 Or 9 For FULL TEXT)
Selecting storage for your AIX system; mainframe storage technology has heavily influenced choices for the RS/6000.
Robidoux, Barbara
MIDRANGE Systems , v5 , n1 , p18(2)
Jan 7 , 1992
ISSN: 1041-8237
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 1211   Line Count: 00096

...generally is the most expensive option and almost always is specified
for the system until itself. For RS/6000 memory, maintenance is a
non-issue. IBM's maintenance fee on a **Model** 550 fully
configured with the **maximum** 512MB of **memory** is the same as
the fee for a 550 with only the standard 64MB of memory, all other things
being equal. Like the system unit...

31/3,K/13 (Item 5 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01377939   Supplier Number: 09634665 (Use Format 7 Or 9 For FULL TEXT)
Fujitsu to market new 9370, 4381 successors internationally.
Computergram International , n1564 , CGI11280004
Nov 28 , 1990
ISSN: 0268-716X
Language: ENGLISH   Record Type: FULLTEXT
Word Count: 284   Line Count: 00019

...its own name. The new machines, claimed to offer 1.4 to nine times the
performance of the M-730s they replace, line up against **IBM**'s new
ES/9221 and ES/9121 **models**; **maximum** main **memory** goes
to 190Mb from 93Mb on the predecessors. The M-740/2, 5, 7, 10 and 20 will
be out in February, the 30 and...

31/3,K/14 (Item 6 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01357744   Supplier Number: 08181898 (Use Format 7 Or 9 For FULL TEXT)

20 billion (pounds sterling)sales keep obituaries away (review of 1989 mainframe market)
Enticknap, Nicholas
Computer Weekly , n1201 , p22(6)
Feb 15 , 1990
ISSN: 0010-4787
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 3377   **Line Count:** 00258

...200J up 600J level, well over 100 mips.
     Also in November Amdahl announced its response to the 3090J launch.
Instead of increasing expanded storage as **IBM** did, Amdahl has
employed new one Mbit Srams to increase main **memory** on all
models. The new **maximum** on the top **models** is one
Gbyte, twice the **IBM** maximum. At the same time, Amdahl followed
IBM's lead and announced the availability of asymmetric central and
expanded storage and channel configurations on all multiprocessors.
     The company became the first on the...

31/3,K/15 (Item 7 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01321895   **Supplier Number: 07335960 (Use Format 7 Or 9 For** FULL TEXT)
Compaq ups 386 ante with 33-MHz Deskpro.
MIS Week , v10 , n22 , p23(1)
May 29 , 1989
ISSN: 0199-8838
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 874   **Line Count:** 00066

...ISA slots are available in standard configurations.
     "Where the Deskpro 386/33 with maximum memory has six slots available
for option boards, the comparably configured **IBM PS/2 Model**
70-A21 with **maximum memory** has only two available slots,"
Canion said.
     "Even the floor-standing PS/2 Model 80-311 has only five slots
available when configured with maximum...

31/3,K/16 (Item 8 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01321614   **Supplier Number: 07088566 (Use Format 7 Or 9 For** FULL TEXT)
IBM boosts AS-400 line.
Neubarth, Michael
MIS Week , v10 , n9 , p8(1)
Feb 27 , 1989
ISSN: 0199-8838
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 1402   **Line Count:** 00102

...processor and improved memory performance that complements the
processor. The B-70 incorporates 1-Mbit DRAMs with a 65-nanosecond access
time -- "the fastest within **IBM**," a spokesman said.
     Maximum main **memory** for the **Model** B-70 is 96
Mbytes, which equals that of the B-60. Maximum DASD for the B-70 is 38.4
Gbytes, an increase over...

31/3,K/17 (Item 9 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01295942   **Supplier Number: 07330758 (Use Format 7 Or 9 For** FULL TEXT)
Company results.
Computergram International , n1194 , CGI06080021
June 8 , 1989
ISSN: 0268-716X
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 671   **Line Count:** 00048

...front? A top-end "Model 80" has been spotted in beta test in the US, and
there is said to be a model installed at **IBM** Deutschland's
Bo"blingen base that is fitted with 256Mb of **memory** against the 96Mb

current **maximum** on the **Model** 70 - perhaps the Germans are
testing 4M-bit memory chips in the machines.

31/3,K/18 (Item 10 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01289102   **Supplier Number: 07077590 (Use Format 7 Or 9 For** FULL TEXT)
IBM boosts high end of AS-400 line. (product announcement)
Bunker, Ted
Electronic News , v35 , n1747 , p14(1)
Feb 27 , 1989
Document Type: product announcement
ISSN: 0013-4937
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 735   **Line Count:** 00054
Abstract: IBM introduces the high-end AS-400 **model** 70 as well as **memory** enhancements to **boost** the power of the
lower-end machines. Although some users claimed to have experienced difficulty migrating System 36 applications to the
AS-400 because of...
Text:

IBM Boosts High End of AS/400 Line WHITE PLAINS, N.Y. -- **IBM** boosted
the high-end performance of its AS/400 line by 30 percent last week with
the addition of the **model** 70, and offered performance-
boosting memory enhancements for the line's low end, where
some users have complained about problems porting System 36 applications.

31/3,K/19 (Item 11 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01250935   **Supplier Number: 06820205 (Use Format 7 Or 9 For** FULL TEXT)
IBM plans summer uplift for RTs. (two IBM RT PC workstations) (product announcement)
Brennan, Laura
PC Week , v5 , n28 , p6(1)
July 11 , 1988
Document Type: product announcement
ISSN: 0740-1604
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 370   **Line Count:** 00028

...a midlife boost this summer with at least two new models, according to
sources close to the company.
    Typical of the midlife products offered by **IBM**, the new RTs
reportedly will feature enhanced peripherals, such as added storage and
memory capacities, as well as a **boost** in processing speed.
    Two new **models**--a desktop version and a tower
configuration--are slated for introduction July 19, but **IBM's** recent
personnel restructuring may delay the announcement, the sources said.
    The RT PC, developed by IBM's Advanced Engineering Systems
Independent Business Unit, located...

31/3,K/20 (Item 12 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01246172   **Supplier Number: 06864173 (Use Format 7 Or 9 For** FULL TEXT)
IBM boosts PC-DOS, RISC line. (MS-DOS 4.0; reduced-instruction-set computer)
Electronic News , v34 , n1716 , p12(2)
July 25 , 1988
ISSN: 0013-4937
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 1477   **Line Count:** 00112

...from the current 32MB limit in a single file to enable a single file to
be as large as the fixed disk itself -- in the **IBM** world that would
be its 314MB **model.**
    Boosted also is support for expanded **memory** -- supplied
by **IBM** via expanded memory cards, options, or emulation -- above 640
kilobytes (KB) by applications written to the Lotus/Intel/Microsoft
Expanded Memory Specification, 4.0. The...

31/3,K/21 (Item 13 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01240022   **Supplier Number: 06258768 (Use Format 7 Or 9 For** FULL TEXT)
Cumulus 32-bit memory card boosts Model 80's memory by up to 8M bytes. (Cumulus Corp., IBM PS-2 Model 80)
(product announcement)
Spiegelman, Lisa L.
PC Week , v5 , n9 , p20(1)
March 1 , 1988
Document Type: product announcement
ISSN: 0740-1604
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 388   Line Count: 00028
Cumulus 32-bit memory card boosts Model 80's memory by up to 8M bytes. (Cumulus Corp., IBM PS-2 Model 80)
(product announcement)

31/3,K/22 (Item 14 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01236622   **Supplier Number: 06272032 (Use Format 7 Or 9 For** FULL TEXT)
CDC bumps memory, I-O in new 990s. (Control Data Corp.)
Electronic News , v34 , n1695 , p15(1)
Feb 29 , 1988
ISSN: 0013-4937
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 515   Line Count: 00039

...32, 994-31 and 994-32, will replace the earlier 990E and 995E machines
when they become available in August.
    The processors, which compete against **IBM's** 3090 **Models**
180E and 200E, support a **maximum** of 256 MB of **memory,** up from
128 MB. CDC said it is using 256K memory components, instead of 64K units,
to increase capacity.
    The uniprocesor and dual processor Cyber...

31/3,K/23 (Item 15 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01211732   **Supplier Number: 04790144 (Use Format 7 Or 9 For** FULL TEXT)
Herculean Model 60 holds aloft IBM's new micro world. (Personal System-2 Model 60) (Hardware Review)
(evaluation)
Pepper, Jon
PC Week , v4 , n17 , p85(1)
April 28 , 1987
Document Type: evaluation
ISSN: 0740-1604
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 1408   Line Count: 00108

...with IBM's new optical-disk drive when it becomes available.
    For the approximately $1,700 price difference between the Model 50
and Model 60, **IBM** is essentially offering more power, flexibility
and growth capabilities. The Model 60 provides seven expansion slots, vs.
three for the **Model** 50, a **maximum** complement of 15M bytes of
RAM (rather than 7M bytes), the potential to add almost 10 times the
mass storage (185M vs. 20M bytes), and an ample 207-watt power supply...

31/3,K/24 (Item 16 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
(c) 2007 The Gale Group. All rights reserved.
01211731   **Supplier Number: 04790143 (Use Format 7 Or 9 For** FULL TEXT)
The PS-2 Model 50 packs major wallop in a compact frame. (Hardware Review) (evaluation)
Kanzler, Stephen
PC Week , v4 , n17 , p84(1)
April 28 , 1987
Document Type: evaluation
ISSN: 0740-1604
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 919   Line Count: 00068

...much better on the Model 50.
    Slots Wanted
    Both the Model 50 and the Model 60 come equipped with 1M byte of
memory, although the **Model** 50 is limited to a **maximum** of 7M
bytes of total **memory** capacity using **IBM**'s memory-expansion
options. This is primarily due to its limited complement of expansion
slots.
    The area where the two machines differ substantially is in...

 31/3,K/25 (Item 17 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01206623   **Supplier Number: 06095046 (Use Format 7 Or 9 For** FULL TEXT)
IBM hi-res adapter, monitor give more room for windowing.
Brennan, Laura
PC Week , v4 , n47 , p4(1)
Nov 24 , 1987
ISSN: 0740-1604
Language: ENGLISH   **Record Type:** FULLTEXT; ABSTRACT
Word Count: 727   **Line Count:** 00057
Abstract: ...set a new graphics standard for multitasking operations in windowing environments. When used together they
will display resolutions of 1,024 by 768 pixels. The **IBM** PS-2 Display Adapter 8514-A is really two boards clasped
together to work in one expansion slot. The base **model** has 16 colors but **memory** modules can **boost** color capacity to
256 colors from a palette of 256,000. The **IBM** PS-2 Color Display 8514 is a 16-inch analog color monitor that works with
the 8514-A board. The products are targeted at high...

 31/3,K/26 (Item 18 from file: 275) <u>Links</u>
Gale Group Computer DB(TM)
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01011299   **Supplier Number:** 00541158
Who Sells What in CPUs.
IBM User , p30
Aug. , 1983
ISSN: 0261-3654
Language: ENGLISH   **Record Type:** ABSTRACT
Abstract: The CPU market is constantly changing. The **IBM** Systems User's survey presents a snapshot of the market in
August, 1983. **Model** number, MIPS, **maximum** channel configuration, **maximum memory** configuration, base price and
operating systems are given for Amdahl, BASF, British Olivetti, ICL, NAS, and **IBM**.

 31/3,K/27 (Item 1 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
(c) 2007 The Gale Group. All rights reserved.
01622733   **Supplier Number:** 48360791 **(USE FORMAT 7 FOR FULLTEXT)**
Zitel Corporation Announces New Vice President of Worldwide Sales
PR Newswire , p N/A
March 16 , 1998
Language: English   **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 487

...international sales at Zitel. Before
    coming to Zitel, Steinmayer worked for Cambex Corporation (OTC:
    CBEX), where he was vice president of marketing, and IBM (NYSE:
    IBM), where he held marketing and sales positions.

    About Zitel Corporation

    Zitel Corporation is an Information Technology company specializing
    in advanced **memory** algorithms, systems **optimization**
, and **modeling**
    and search technology. The company employs these core competencies
    in three related lines of business: multi-platform and multi-system
    performance measurement and modeling software...

 31/3,K/28 (Item 2 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
(c) 2007 The Gale Group. All rights reserved.
01136944   **Supplier Number:** 41184785 **(USE FORMAT 7 FOR FULLTEXT)**

AMERICAN INTERNATIONAL INTRODUCES FIRST 8 MB ADD-IN MEMORY FOR AS/400 MODELS B-10, B-20
News Release , p 1
Feb 22 , 1990
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 502

...and one AI/4104 4 Mb memory board are
    needed to bring the B-10 up to its full capacity of 16 Mb. Three 4Mb
    IBM
memory boards are needed to obtain the same memory capacity.

        The economies are even more dramatic in the newest **Model**
B-20,
    which has a **maximum memory**
capacity of 28 Mb. This can now be
    achieved with a total of only four add-in boards--two AI4104DD memory
    boards and two 4...

 31/3,K/29 (Item 3 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
(c) 2007 The Gale Group. All rights reserved.
01096133   **Supplier Number: 40643021 (USE FORMAT 7 FOR FULLTEXT)**
MICROSOFT QUICK 2.0 SHIPS – UPDATE OFFERS REVOLUTIONARY TECHNOLOGY FOR C PROGRAMMERS
News Release , p 1
Jan 12 , 1989
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 1073

...small, medium, compact, large and huge) from
    within the integrated environment. The compiler also supports the
    NEAR, FAR and HUGE keywords, allowing users to mix **memory**
models for
    maximum efficiency in **memory** use.

    System Requirements, Pricing and Availability

    Minimum system requirements for Microsoft QuickC Compiler version 2.0
    are an **IBM**
(R) Personal Computer or compatible with 512K available
    user memory, DOS 2.1 or higher, and either two double-sided 5.25-inch
    drives or...

 31/3,K/30 (Item 4 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
(c) 2007 The Gale Group. All rights reserved.
01096132   **Supplier Number: 40643020 (USE FORMAT 7 FOR FULLTEXT)**
MICROSOFT QUICKC 2.0 SHIPS – UPDATE OFFERS REVOLUTIONARY TECHNOLOGY FOR PROGRAMMERS
News Release , p 1
Jan 12 , 1989
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 1039

...small, medium, compact, large and huge) from
    within the integrated environment. The compiler also supports the
    NEAR, FAR and HUGE keyboards, allowing users to mix **memory**
models for
    maximum efficiency in **memory** use.

    Systems Requirements, Pricing and Availability

    Minimum systems requirements for Microsoft QuickC compiler version
    2.0 are an **IBM**
 Personal Computer or compatible with 512K available
    user memory, DOS 2.1 or higher, and either two double-sided 5.25-inch

drives or one...

31/3,K/31 (Item 5 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
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01068919   **Supplier Number: 40334952 (USE FORMAT 7 FOR FULLTEXT)**
FLORIDA CORPORATION SELECTS SAN FRANCISCO COMPUTER FAIRE FOR IBM PRODUCT INTRODUCTION
PR Newswire , p 1
March 25 , 1988
Language: English   **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 409

...2 operating system, or stay
    with the original DOS system.

    In addition to showing their current products, Boca will introduce
    TOPHAT II which will backfill **IBM** AT, XT286 and compatible
models
    system **memory** to the DOS **maximum**
of 640K (kilobytes). The new board
    is designed to operate at higher CPU speeds, a common concern among
    AT compatibles that have been speeded up...

31/3,K/32 (Item 6 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
(c) 2007 The Gale Group. All rights reserved.
01037676   **Supplier Number: 40017020 (USE FORMAT 7 FOR FULLTEXT)**
IBM'S PERSONAL SYSTEM/2 FAMILY FEATURES FOUR HIGH-PERFORMANCE SYSTEMS
PR Newswire , p N/A
April 2 , 1987
Language: English   **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 1358

...graphics capabilities.

    In addition, the new systems eliminate system setup switches, while a
    new system board design accommodates up to a sixfold increase in the
    maximum amount of easily installable **memory** in some
models. The
    system power supply is capable of adjusting the voltages in foreign
    countries.

    Powerful New Graphics

    IBM Personal System/2 incorporates enhanced integrated graphics
    functions including significantly improved text, expanded colors with
    up to 256 out of a palette of more than...

31/3,K/33 (Item 7 from file: 621) <u>Links</u>
Gale Group New Prod.Annou.(R)
(c) 2007 The Gale Group. All rights reserved.
01004910   **Supplier Number: 39547173 (USE FORMAT 7 FOR FULLTEXT)**
IBM SYSTEM/38 ADDS OFFICE SYSTEMS CAPABILITIES, NEW MID-RANGE PROCESSOR
PR Newswire , p N/A
June 18 , 1985
Language: English   **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 790

...relational data base. Users can now read data from up to 32
    physical files as if they were actually one file.

- 3 -
                    Other Features

The **IBM**
System/38 5381 model 6 has been enhanced with an additional
2MB increment of main **memory** -- to a new 6MB **maximum**
. The new **model**
provides growth capability for 5381 customers who have additional
memory requirements but don't need the internal performance of the
5382 series. Also announced were...

31/3,K/34 (Item 1 from file: 47) <u>Links</u>
Gale Group Magazine DB(TM)
(c) 2007 The Gale group. All rights reserved.
03479097   **Supplier Number: 09691369 (USE FORMAT 7 OR 9 FOR FULL TEXT)**
IBM fiber breaks data center barrier. (the Enterprise Systems Connection Architecture fiber-optic connectivity architecture)
Bunker, Ted
Datamation , v36 , n23 , p85(2)
Dec 1 , 1990
ISSN: 1062-8363
Language: ENGLISH   Record Type: FULLTEXT; ABSTRACT
Word Count: 1601   Line Count: 00130

...of a 10MBps direct connection to current direct access storage device
(DASD) systems, Strolis says. While connected DASD 3990 controllers are
limited to 4.2MBps **maximum** throughput, **IBM** says cache
memory supplied with the high-end (**model** 3) controllers can
collect data at the 10MBps rate. **IBM** declines to speculate on when
it may improve direct-connect throughput.
    IBM says it will make available the ESCON adapters for its 3990 DASD
controllers...

31/3,K/35 (Item 2 from file: 47) <u>Links</u>
Gale Group Magazine DB(TM)
(c) 2007 The Gale group. All rights reserved.
02948751   **Supplier Number: 04790835 (USE FORMAT 7 OR 9 FOR FULL TEXT)**
Herculean model 60 holds aloft IBM's new micro world. (includes related article on DOS 3.x) (IBM Personal System-2 computer) (evaluation)
Pepper, Jon
PC Week , v4 , p85(1)
April 28 , 1987
Document Type: evaluation
Language: ENGLISH   Record Type: FULLTEXT
Word Count: 1408   Line Count: 00108

...with IBM's new optical-disk drive when it becomes available.
    For the approximately $1,700 price difference between the Model 50
and Model 60, **IBM** is essentially offering more power, flexibility
and growth capabilities. The Model 60 provides seven expansion slots, vs.
three for the **Model** 50, a **maximum** complement of 15M bytes of
RAM (rather than 7M bytes), the potential to add almost 10 times the
mass storage (185M vs. 20M bytes), and an ample 207-watt power supply...

31/3,K/36 (Item 3 from file: 47) <u>Links</u>
Gale Group Magazine DB(TM)
(c) 2007 The Gale group. All rights reserved.
02948750   **Supplier Number: 04790834 (USE FORMAT 7 OR 9 FOR FULL TEXT)**
The PS-2 model 50 packs major wallop in a compact frame. (IBM Personal System-2 computer) (evaluation)
Kanzler, Stephen
PC Week , v4 , p84(1)
April 28 , 1987
Document Type: evaluation
Language: ENGLISH   Record Type: FULLTEXT
Word Count: 919   Line Count: 00068

...much better on the Model 50.
    Slots Wanted
    Both the Model 50 and the Model 60 come equipped with 1M byte of
memory, although the **Model** 50 is limited to a **maximum** of 7M

bytes of total **memory** capacity using **IBM**'s memory-expansion
options. This is primarily due to its limited complement of expansion
slots.
    The area where the two machines differ substantially is in...

31/3,K/37 (Item 4 from file: 47) <u>Links</u>
Gale Group Magazine DB(TM)
(c) 2007 The Gale group. All rights reserved.
02809879   **Supplier Number: 04097528** (USE FORMAT 7 OR 9 FOR FULL TEXT)
Two strategic systems are readied by IBM: upgraded S-36 mini to have more power for department role; main memory to double.
Garretson, Rob
PC Week ; v3 , p1(2)
Jan 14 , 1986
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 698   **Line Count:** 00056

...36 models degrades the machine's performance. The second disk controller
will solve this problem by allowing simultaneous disk access by multiple
users, they added.
    Maximum memory on the new **model** will be 4M
bytes, sources said, compared with the 1.75M-byte capacity of the current
high-end System/36.
    IBM will also add a faster processor, fully compatible with
the smaller System/36 models.
    IBM will also introduce a new release of the System/36...

31/3,K/38 (Item 5 from file: 47) <u>Links</u>
Gale Group Magazine DB(TM)
(c) 2007 The Gale group. All rights reserved.
02365024   **Supplier Number: 02738122** (USE FORMAT 7 OR 9 FOR FULL TEXT)
Low-end action at IBM; a sweeping range of new products is helping IBM meet competition from DEC, HP, and AT&T.
Verity, John W.
Datamation , v29 , p75(2)
May , 1983
CODEN: DTMNA
Language: ENGLISH   **Record Type:** FULLTEXT
Word Count: 1039   **Line Count:** 00081

...year-old line with a model 4956 processor that is said to offer internal
speeds 20% faster than its predecessor, the 4955 F. The new **model**
also ups the **maximum** series/1 main **memory** capacity to a full
megabyte.
    Meanwhile, **IBM** introduced a new software package designed to
manage remote Series/1 processors from a central site. This is expected to
appeal to large commercial customers...

31/3,K/39 (Item 1 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
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02051798   **Supplier Number: 43742778 (USE FORMAT 7 FOR FULLTEXT)**
NEW F MODELS FORTIFY THE LINE
Report on IBM , v 10 , n 13 , p N/A
March 31 , 1993
Language: English   **Record Type:** Fulltext
Document Type: Newsletter ; Trade
Word Count: 1412

...TPC-C test is designed to more closely simulate real world operations.
Test results for the more powerful three-processor F90 and four-processor
F95 **models** weren't released by **IBM**.
    Maximum main **memory** is greater for several of these
machines too. The F50 now accepts up to 192 M RAM, and the F60 can take up
to

31/3,K/40 (Item 2 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
01715576   **Supplier Number: 42782705 (USE FORMAT 7 FOR FULLTEXT)**
IBM revamps AS/400
Computer Product Update , p N/A
Feb 28 , 1992
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 612

...an office environment. The three 9404 models are slightly larger and can
also operate in an office. The seven 9406 models are mounted in racks.
    IBM AS/400 **models**

Model	Power1	Max users2	Ram	Disk
		Ascii 5250	MB	GB
				Maximum

9402:
E02 1.5 12   14 24 1.97
E04 1.9 48   42 24 3.95
E06 2.6 66   68 40 3.95...

31/3,K/41 (Item 3 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
01473939   **Supplier Number: 42027031 (USE FORMAT 7 FOR FULLTEXT)**
486SX MODELS 90 AND 95 PROTECT CUSTOMERS' INVESTMENT
Report on IBM , v 8 , n 17 , p N/A
April 24 , 1991
Language: English   **Record Type:** Fulltext
Document Type: Newsletter ; Trade
Word Count: 922

...the downward migration of the upgradable XP architecture. Prices range
from $8,345 to $17,195 for the new 486SX-equipped models, including 4M RAM.
    IBM also cut prices on existing **Model** 90/95 machines and
boosted standard **RAM** to 8M. The list price of many other
models were also cut in response to sluggish sales, and some models have
been dropped.
    The trend...

31/3,K/42 (Item 4 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
01119034   **Supplier Number: 40844846 (USE FORMAT 7 FOR FULLTEXT)**
NEWS - EDINBURGH CONFERENCE FOCUSES ON ELECTRONIC BANKING MARKETPLACE
Electronic Banking & Finance , v 6 , n 5 , p N/A
July , 1989
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 1015

...models is priced from $10 000 to $18 000 and is said to approach the
speed and power of "modest minicomputers".
    Each of the new **models** has a **maximum** of 1.3 gigabytes of
memory, which makes it faster than any other desktop on the market,
say Compaq sources. **IBM** is expected to update its desktop machines,
but Compaq has taken the lead in that direction by using

31/3,K/43 (Item 5 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
01113311   **Supplier Number: 40822258 (USE FORMAT 7 FOR FULLTEXT)**
IBM AS/400 'MODEL 80' SPOTTED IN BETA TEST IN THE US
Computergram International , n 1193 , p N/A

June 8 , 1989
Language: English   **Record Type:** Fulltext
Document Type: Newswire ; Trade
Word Count: 70
(USE FORMAT 7 FOR FULLTEXT)
Text:

...front? A top-end "Model 80" has been spotted in beta test in the US, and
there is said to be a model installed at **IBM** Deutschland's
Bo"blingen base that is fitted with 256Mb of **memory** against the 96Mb
current **maximum** on the **Model** 70 -perhaps the Germans are
testing 4M-bit memory chips in the machines.

31/3,K/44 (Item 6 from file: 636) <u>Links</u>
Gale Group Newsletter DB(TM)
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01079303   **Supplier Number:** 40690558 **(USE FORMAT 7 FOR FULLTEXT)**
BIG BLUE UNWRAPS AS/400 B70; BOOSTS MEMORY FOR ENTRY MODELS
Report on IBM , v 6 , n 8 , p N/A
Feb 22 , 1989
Language: English   **Record Type:** Fulltext
Document Type: Newsletter ; Trade
Word Count: 181
BIG BLUE UNWRAPS AS/400 B70; BOOSTS MEMORY FOR ENTRY MODELS

31/3,K/45 (Item 1 from file: 148) <u>Links</u>
Gale Group Trade & Industry DB
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03470484   **Supplier Number:** 06298756 (USE FORMAT 7 OR 9 FOR FULL TEXT)
Florida corporation selects San Francisco Computer Faire for IBM product introduction. (Boca Research Inc.)
(product announcement)
PR Newswire , 0325FL3
March 25 , 1988
Document Type: product announcement
Language: ENGLISH
Record Type: FULLTEXT
Word Count: 426   **Line Count:** 00033

...2 operating system, or stay with the original DOS system.
    In addition to showing their current products, Boca will introduce
TOPHAT II which will backfill **IBM** AT, XT286 and compatible
models' system **memory** to the DOS **maximum** of 640K
(kilobytes). The new board is designed to operate at higher CPU speeds, a
common concern among AT compatibles that have been speeded up...

31/3,K/46 (Item 1 from file: 16) <u>Links</u>
Gale Group PROMT(R)
(c) 2007 The Gale Group. All rights reserved.
02413851   **Supplier Number:** 43176459 **(USE FORMAT 7 FOR FULLTEXT)**
IBM goes Hollywood
Electronic Engineering Times , p 16
July 27 , 1992
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 404

...the introduction of the PVS Model 4 Server. The parallel-processing
system incorporates 32 Intel i860XP CPUs and as much as 2.5 Gbytes of
memory. In addition, the **maximum** system **memory** in PVS
models 1, 2 and 3 was increased from 1.5 to 2.5 Gbytes.
    IBM also extended the multiuser capability of PVS servers to
handle up to eight users simultaneously.
    In the software arena, IBM introduced an improved version of...

31/3,K/47 (Item 2 from file: 16) <u>Links</u>
Gale Group PROMT(R)
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01624848   Supplier Number: 42006302
PC lineup set for 486 'SX'
Computerworld , p 1
April 15 , 1991
Language: English   **Record Type:** Abstract
Document Type: Magazine/Journal; Tabloid ; Trade
Abstract:

...reach its summit in 1991 and the 486SX will replace it, a natural
migration. Machines are expected to be forthcoming from Everex Systems, AST
Research, **IBM**, Compaq Computer, Dell Computer and Advanced Logic
Research. AST Research will reportedly supply four desktop 486SX-based
models, all featuring 4 Mbytes of **memory**, which can be
boosted to 16 Mbytes on the motherboard and 80 Mbytes total via
external expansion. Everex's two 486SX-based systems will reportedly
operate as swift as...

31/3,K/48 (Item 3 from file: 16) <u>Links</u>
Gale Group PROMT(R)
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01105959   **Supplier Number: 41240782 (USE FORMAT 7 FOR FULLTEXT)**
HDS Adds Two CPUs To IBM-Compatible Line
Electronic News (1991) , p 17
March 26 , 1990
Language: English   **Record Type:** Fulltext
Document Type: Magazine/Journal ; Trade
Word Count: 308
At the same time, HDS **boosted** the **maximum memory**
configurations for all dyadic intermediate **models** from 256MB to
512MB of storage, and pushed up the schedule to ship its version of
IBM's Extended Systems Architecture on its low-end to mid-range
systems.
    As expected (EN, March 19), HDS stoked its bid for the lowend and...

31/3,K/49 (Item 1 from file: 813) <u>Links</u>
PR Newswire
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1134096   SFF011
Zitel Corporation Announces Management Changes
Date: August 1, 1997   06:30 EDT   **Word Count:** 729
...Internet service provider. In addition to management positions at
CompuServe, Inc. and CyberSource Corporation, Mr. Hogan spent the first 12
years of his career at **IBM Corporation**, where he held several
senior sales and marketing positions.
    Zitel Corporation is an Information Technology company that specializes
in advanced **memory** algorithms, systems **optimization** and
modeling and search technology. The Company employs these core
competencies in three related lines of business: single-system and
multi-system measurement and modeling software used...

31/3,K/50 (Item 1 from file: 634) <u>Links</u>
San Jose Mercury
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04534895
SEND IN THE CLONES
SAN JOSE MERCURY NEWS (SJ) - Sunday, May 1, 1988
By: JIM BARTIMO, Mercury News Computing Editor
Edition: Morning Final **Section:** Computing **Page:** 1F
Word Count: 1345
...disadvantage: a 40MB hard disk compared with the Model 80's 44MB one.
    Dell's System 400 has a faster central processing chip than the
IBM Model 60, can hold a **maximum** of 16MB of **RAM**
to the **Model** 60's 15MB and has one more expansion slot, but it, too,
has the smaller hard disk.
    Corporate users of **IBM**'s PS/2 who buy in large volume are already
getting about a $500 discount, and IBM will probably cut its prices for
individual buyers...